Compal confidential

Schematics Document

Mobile Arrandale rPGA989 with Intel PCH(Ibex Peak-M) core logic

2009-11-05

REV 1.0

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

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Title: Cover Sheet		
Size: Custom	Document Number: Calpella_UMA_LA4106P	Rev: 1.0
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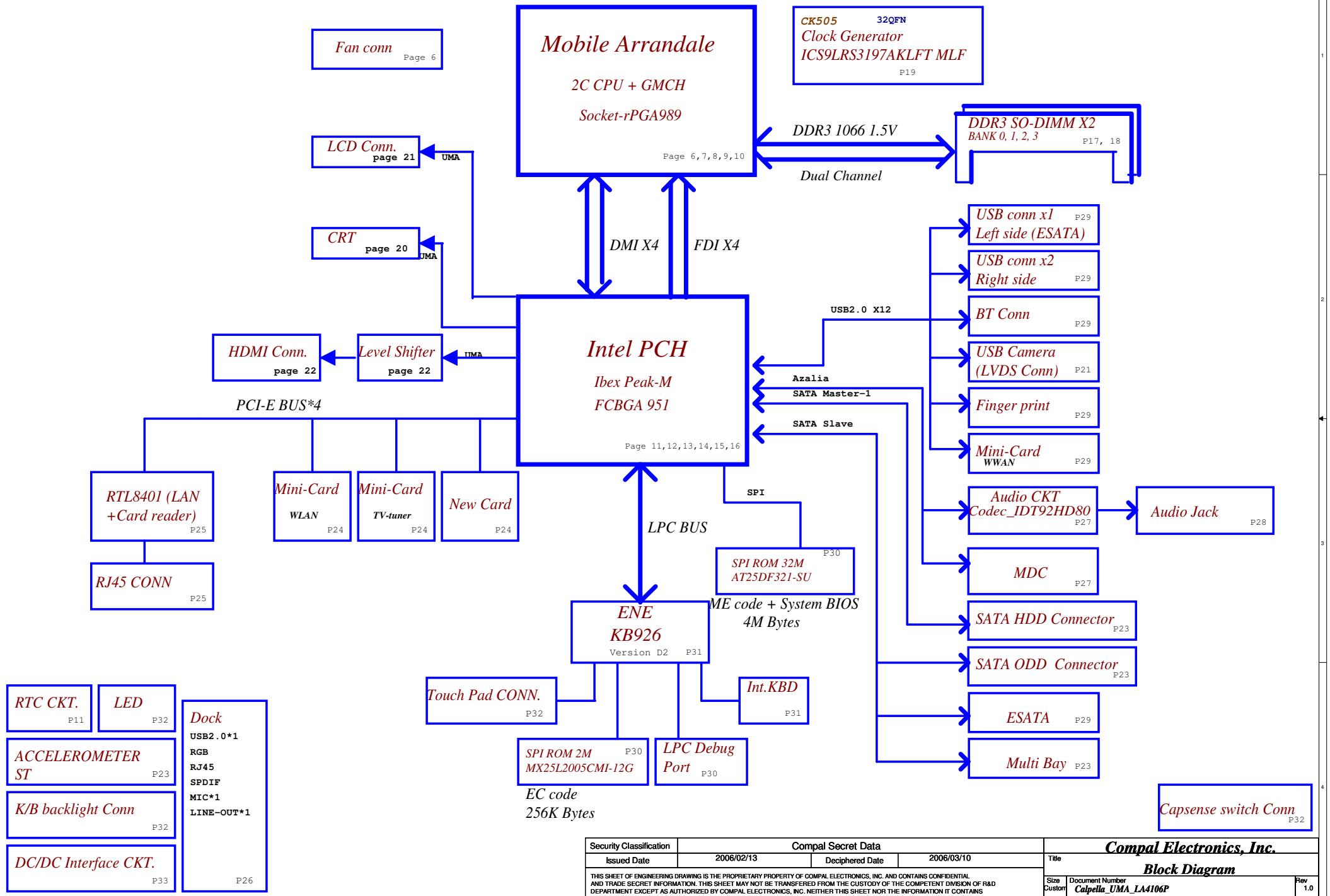
Compal confidential

Calpella Consumer 14" UMA



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.			
Title: Block Diagram			
Size: Custom	Document Number: Calpella_UMA_LA4106P		Rev: 1.0
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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +1.05VS +1.5VS_CPU
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
PA@ :	Only For PA (With Capacitor sensor)
OPP@ :	For POWER BUTTON (NO CAP SERSOR)
DEBUG@ :	For DEBUG

USB assignment:

USB-0	Left side(with ESATA)
USB-1	Right side
USB-2	Right side
USB-3	Dock
USB-4	Camera
USB-5	MiniCard(WLAN)
USB-6	X (HM55 don't support)
USB-7	X (HM55 don't support)
USB-8	MiniCard(WWAN)
USB-9	New Card
USB-10	X
USB-11	Finger Printer
USB-12	Bluetooth
USB-13	X

PCIe assignment:

PCIe-1	WWAN
PCIe-2	WLAN
PCIe-3	RTL8401 Combo
PCIe-4	New card
PCIe-5	X
PCIe-6	X
PCIe-7	X (HM55 don't support)
PCIe-8	X (HM55 don't support)

SATA assignment:

SATA0	HDD
SATA1	ODD
SATA2	X (HM55 don't support)
SATA3	X (HM55 don't support)
SATA4	ESATA
SATA5	Multi Bay

SMBUS Control Table

	SOURCE	XDP	BATT	Thermal Sensor	SODIMM	CLK GEN	WWAN	WLAN	M93 Thermal Sensor	Cap sensor board	NEW CARD	G sensor	
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	X	X	X	X	X	X	V	X	X	+3VL
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	X	X	X	X	X	X	X	X	+3VALW
SMBCLK SMBDATA	PCH	X	X	X	V	V	V	V	X	X	V	V	+3VS/+3VALW
SML0CLK SML0DATA	PCH	X	X	X	X	X	X	X	X	X	X	X	+3VALW
SML1CLK SML1DATA	PCH	X	X	X	X	X	X	X	X	X	X	X	
		VCCP			+3VS	+3VS	+3VS @+3VALW	+3VS @+3VALW		+3VL	+3VS	+3VS	

CONNECTED

PCH I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0
G sensor	1D	0 0 0 1 1 1 0 1

EC I2C / SMBUS1 ADDRESSING

DEVICE	HEX	ADDRESS
Smart Battery		
Cap Sensor board		

ZZZ DAZ0BI00100 PA@

ZZZ DAZ0BI00400 OPP@

PCB: DA60000F400
PA@: DAZ0BI00600 (w/o SIM daoughter/B)
OPP@: DAZ0BI00400

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Title: Notes List

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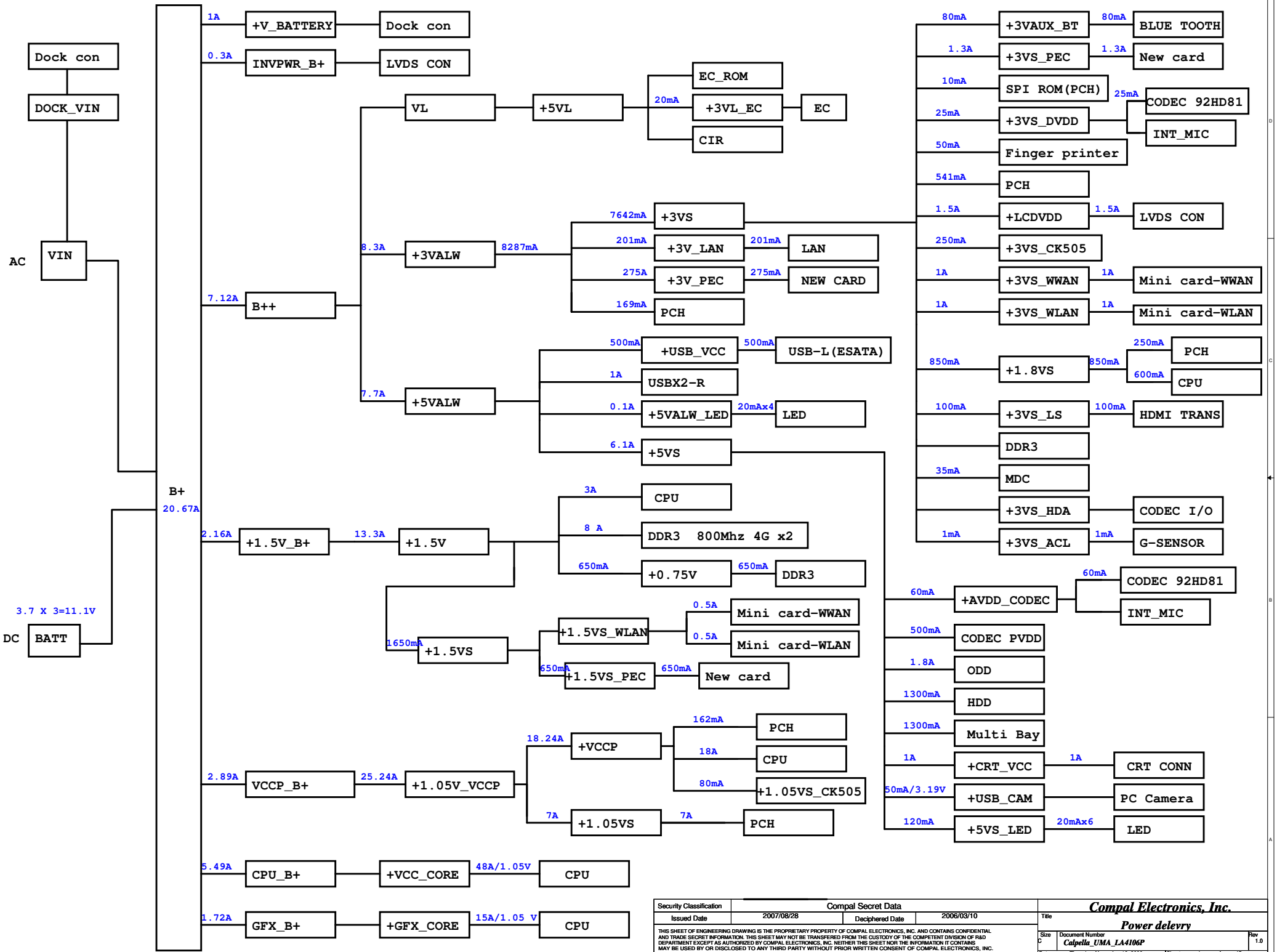

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Title: Power delevry

Size	Document Number	Rev
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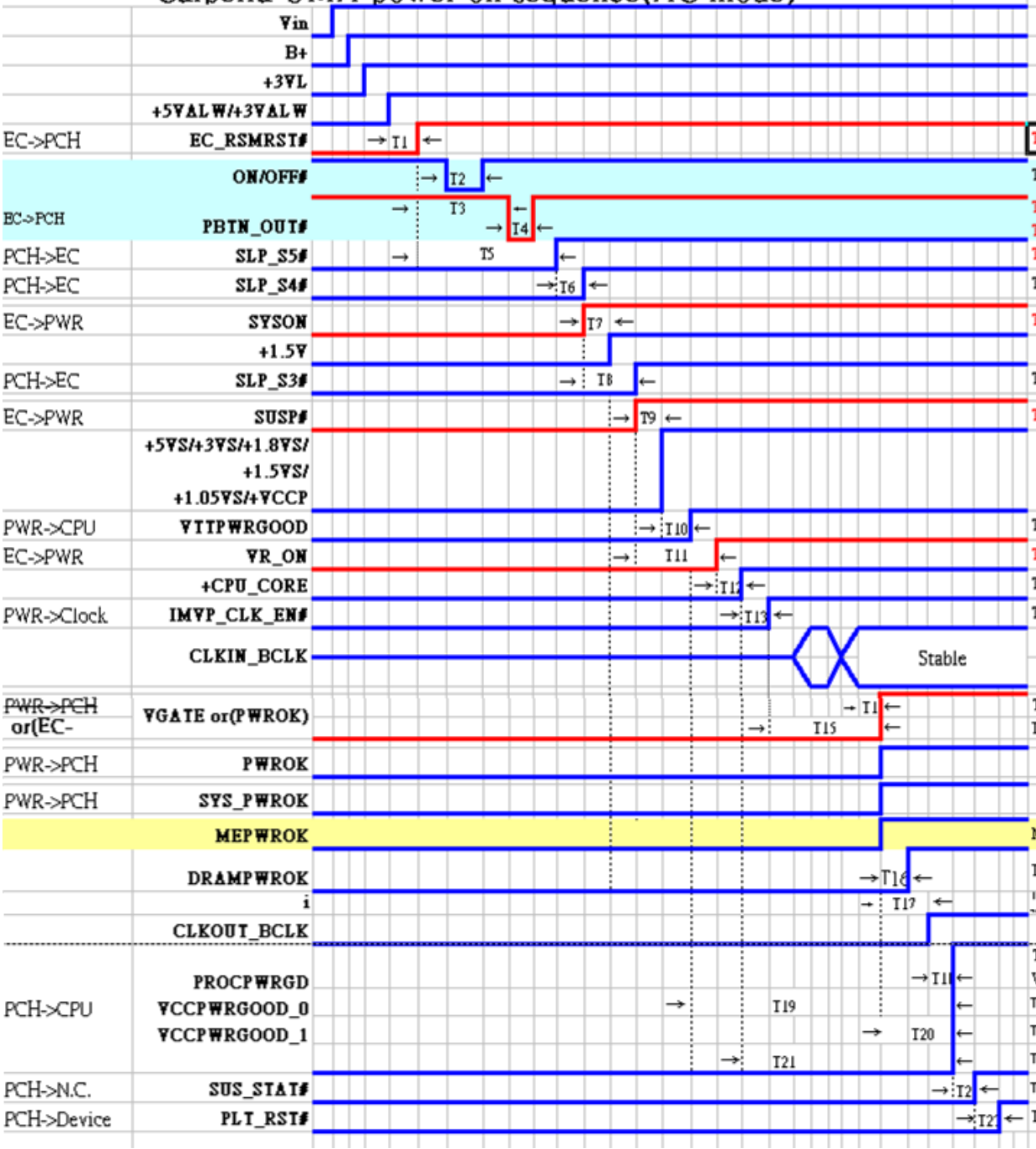
Calpella UMA power on sequence(AC mode)

98.03.03.



	Spec	define	min	Max
	T1, >10ms , +3VALW to RSMRST#	T03	10 ms	-
	T2, User define			
	T3>150ms, T4,100ms			
	T5, >100ms,RSMRST# to SLP_S5#	T07	100 ms	-
	T6,>30us, SLP_S5# to SLP_S4#	T08	30 us	-
	T7,10ms, SLP_S3# to SYSON			
	T8,>30us, SLP_S4# to SLP_S3#	T09	30 us	-
	T9,20ms, SLP_S3# to SUSP#			
	T10,VCCP stable to VTTPWRGOOD assertion to the pro	T13	0.0001 ms	500 ms
	T11>130ms , SLP_S3# to VR_ON	T16	99 ms	-
	T12,Intel MVP soft start ramp-up time of +VCC_CORE	T17	-	3 ms
	T13,Duration Intel MVP V-boot, timing set by IMVP6.5	T18	10 us	100 us
	T14,CLKIN_BCLK stable to VGATE assertion	T19	1 ms	-
	T15 IMVP_CLK_EN# to VGATE assert. Timing set by MVI	T20	3 ms	20 ms
	MEPWROK connecto to PWROK(iAMT disable)			
	T16.+1.5V stable to DRAMPWROK assertion.Timing set by	T22	100 ns	-
	T17.SYS_PWROK/PCH_PWROK assertion to DRAMPWROK	T23	1 ms	-
	T18,CLKOUT_BCLK stable to VCCPWRGOOD_0 ~ VCCPWRGOOD_1 assertion to Processor . Timing set	T24	10 BCKS	1 ms
	T19.VTTPWRGD to VCCPWRGOOD assertion. Timing set by PCH	T25	1 ms	-
	T20.VGATE assertion to VCCPWRGOOD assertion. Timing by PCH	T26	1 ms	100 ms
	T21.VCORE stable to VCCPWRGOOD assertion	T27	0.05 ms	650 ms
	T22.VCCPWRGOOD to SUS_STAT# .timing default = 1ms	T28	0.03 ms	-
	T23.SUS_STAT# to PLTRST# . timing set by PCH	T29	60 us	-

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Title: **Notes List**

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Layout rule 10mil width trace length < 0.5", spacing 20mil

JCPU1B

MISC
R1 20_0402_1% COMP3 AT23
R3 20_0402_1% COMP2 AT24
R5 49.9_0402_1% COMP1 G16
R7 49.9_0402_1% COMP0 AT26
PAD T1 TP_SKTOCC# AH24 SKTOCC#

THERMAL
H_CATERR# AK14 CATERR#
14 H_PECI R10 H_PECI_ISO AT15 PECI
40 H_PROCHOT# H_PROCHOT# AN26 PROCHOT#
14 H_THERMTRIP# H_THERMTRIP# AK15 THERMTRIP#

PWR MANAGEMENT
PAD T73 H_CPURST#_R AP26 RESET_OBS#
13 H_PM_SYNC R20 H_PM_SYNC_R AL15 PM_SYNC
H_CPUPWRGD R21 SYS_AGENT_PWROK AN14 VCCPWRGOOD_1
14 H_CPUPWRGD R23 VCCPWRGOOD_0 AN27 VCCPWRGOOD_0
VDDPWRGOOD_R AK13 SM_DRAMPWROK
38 VCCP_POK R1216 2K_0402_1% AM15 VTTPWRGOOD
1.5K_0402_1% R1217
PAD T74 H_PWRGD_XDP_R AM26 TAPPWRGOOD
14 BUF_PLT_RST# R26 PLT_RST#_R AL14 RSTIN#
1.5K_0402_1%
R28 750_0402_1%

Design guide 1.11update,PLTRST series resittor 1.5K, PL resistor 750 ohm

CLOCKS
BCLK A16 CLK_CPU_BCLK → CLK_CPU_BCLK 14
BCLK# B16 CLK_CPU_BCLK# → CLK_CPU_BCLK# 14
BCLK_ITP AR30
BCLK_ITP# AT30
PEG_CLK E16 CLK_EXP → CLK_EXP 12
PEG_CLK# D16 CLK_EXP# → CLK_EXP# 12
DPLL_REF_SSCLK A18
DPLL_REF_SSCLK# A17 eDP

DDR3 MISC
SM_DRAMRST# F6 SM_DRAMRST#
SM_RCOMP[0] AL1 SM_RCOMP0
SM_RCOMP[1] AM1 SM_RCOMP1
SM_RCOMP[2] AN1 SM_RCOMP2
PM_EXT_TS#[0] AN15 PM_EXTTS#0
PM_EXT_TS#[1] AP15 PM_EXTTS#1 R14 T63 PAD 0_0402_5% → PM_EXTTS#1_R 17,18
from DDR

JTAG & BPM
PRDY# AT28
PREQ# AP27 XDP_PREQ#
TCK AN28 XDP_TCK
TMS AP28 XDP_TMS
TRST# AT27 XDP_TRST#
TDI AT29 XDP_TDI_R
TDO AR27 XDP_TDO_R
TDI_M AR29 XDP_TDI_M
TDO_M AP29 XDP_TDO_M
DBR# AN25 XDP_DBRESET# → XDP_DBRESET# 13
BPM#[0] AJ22
BPM#[1] AK22
BPM#[2] AK24
BPM#[3] AJ24
BPM#[4] AJ25
BPM#[5] AH22
BPM#[6] AK23
BPM#[7] AH23

+VCCP
PM_EXTTS#0 R27 10K_0402_5%
PM_EXTTS#1 R29 10K_0402_5%

IC;AUB_CFD_rPGA,R1P0
CONN@

XDP Connector

+VCCP
XDP_TDI @R2 51_0402_1%
XDP_TMS @R4 51_0402_1%
XDP_PREQ# @R6 51_0402_1%
XDP_TDO R8 51_0402_1%
This shall place near CPU
XDP_TCK @R9 51_0402_1%

JTAG MAPPING
XDP_TDI_R R30 0_0402_5% XDP_TDI
XDP_TDO_M @R32 0_0402_5% XDP_TDO
R34 0_0402_5%
XDP_TDI_M @R37 0_0402_5%
XDP_TDO_R R38 0_0402_5%
XDP_TRST# R39 51_0402_1%

+3VS
XDP_DBRESET# R603 1K_0402_5%

Processor Pullups

+VCCP
H_CATERR# R35 49.9_0402_1%
H_CPURST#_R @R36 68_0402_5%
H_PROCHOT# R11 68_0402_5%

DDR3 Compensation Signals

SM_RCOMP0 R40 100_0402_1%
SM_RCOMP1 R41 24.9_0402_1%
SM_RCOMP2 R42 130_0402_1%

Layout Note:Please these resistors near Processor

+1.5V
@R1205 0_0402_5%
R12 1K_0402_1%
Q104
SM_DRAMRST# → DRAMRST# 17,18
BSS138_NL_SOT23-3
R15 100K_0402_5%
PCH_DDR_RST 14
C12 470P_0402_50V7K
@C1438 @C1439 @C1440
0.1U_0402_16V4Z
0.1U_0402_16V4Z
0.1U_0402_16V4Z

1103_Add 0.1uF for DRAMRST#.

1.5VSCPU_DRAM_PWRGD 39
R1208 1.5K_0402_1%
1.5VSCPU_DRAM_PWRGD
+1.5V
@R384 1.1K_0402_1%
R1209
13 PM_DRAM_PWRGD
PM_DRAM_PWRGD
0_0402_5%
VDDPWRGOOD_R
@R383 3K_0402_1%
R1218 750_0402_1%

+3VALW
VCCP_POK
U57
NC7SZ08P5X_NL_SC70-5

PWM Fan Control circuit

1105_Add R597.

+5VS
R597 0_0603_5%
JP2
D48 RB751V_SOD323
C3 4.7U_0805_10V4Z
C295 0.1U_0402_16V4Z
GND
GND
ACES_88231-02001
CONN@
+FAN
31 FAN_PWM
Q97 SI3456BDV-T1-E3_TSOP6
@D49 RLZ5.1B_LL34

Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

Compal Electronics, Inc.

Title: Auburndale(1/5)-Thermal/XDP

Size	Document Number	Rev
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Layout rule trace length < 0.5"

JCPU1A

DMI

PCI EXPRESS -- GRAPHICS

Intel(R) FDI

IC,AUB_CFD_rPGA,R1P0
CONN@

JCPU1E

RESERVED

IC,AUB_CFD_rPGA,R1P0
CONN@

CRB 0.9 change to GND

CFG Straps for PROCESSOR

CFG0 @R52 1 2 3.01K_0402_1%

PCI-Express Configuration Select	
CFG0	1: Single PEG * 0: Bifurcation enabled

Not applicable for Clarksfield Processor

CFG3 R54 1 2 3.01K_0402_1%

CFG3-PCI Express Static Lane Reversal	
CFG3	1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 ->1, ... *

CFG4 @R53 1 2 3.01K_0402_1%

CFG4-Display Port Presence	
CFG4	1: Disabled; No Physical Display Port * attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7 @R55 1 2 3.01K_0402_1%

Only temporary for early CFD samples (rPGA/BGA)

Only for pre ES1 sample

CFG7
NW33 PD 3.01K on CFG7 for PCIE Jitter
NW41 don't staff

Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

Compal Electronics, Inc.

Title: Auburndale(2/5)-DMI/PEG/FDI

Size	Document Number	Rev
Custom	Calpella_UMA_LA4106P	1.0

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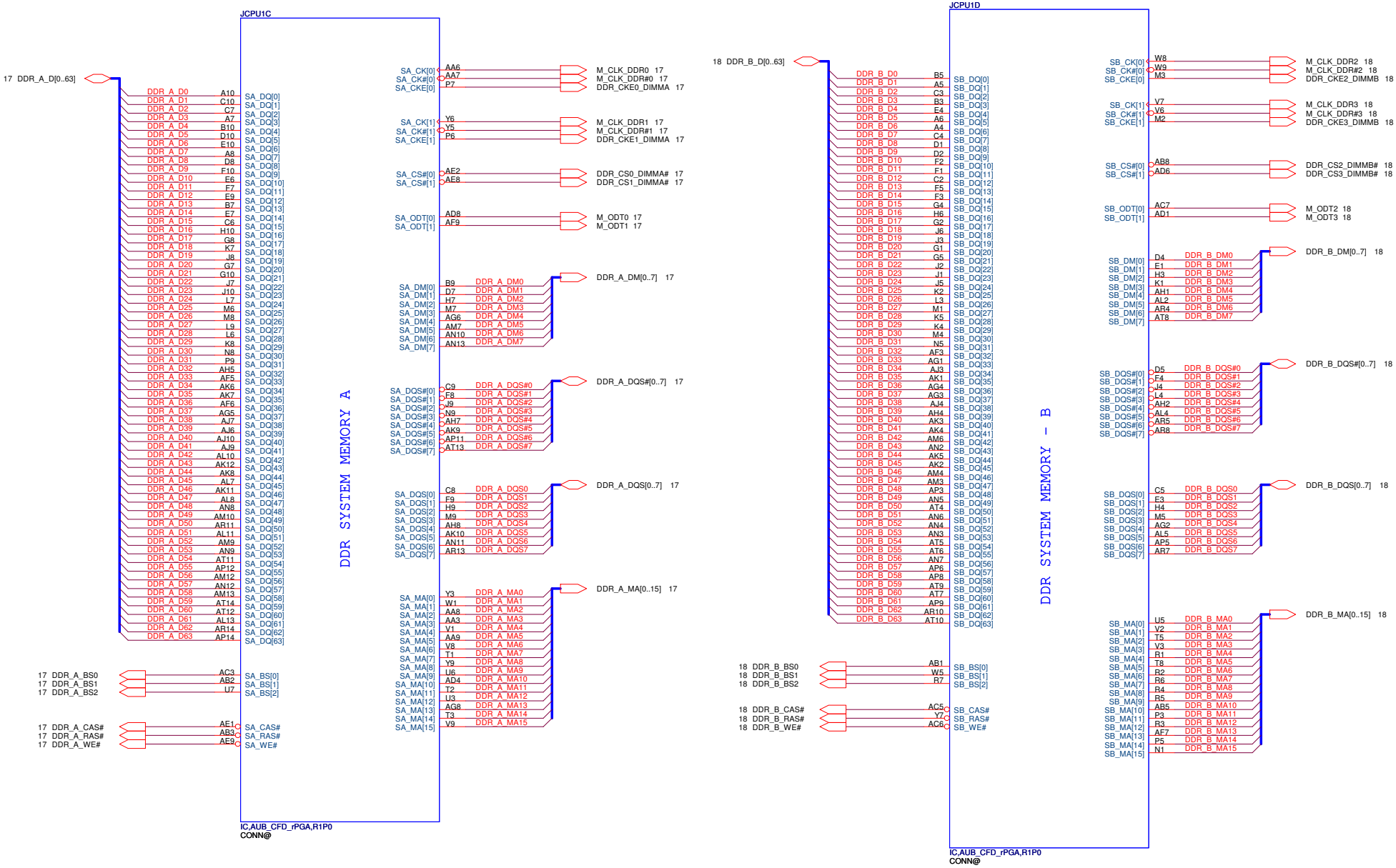
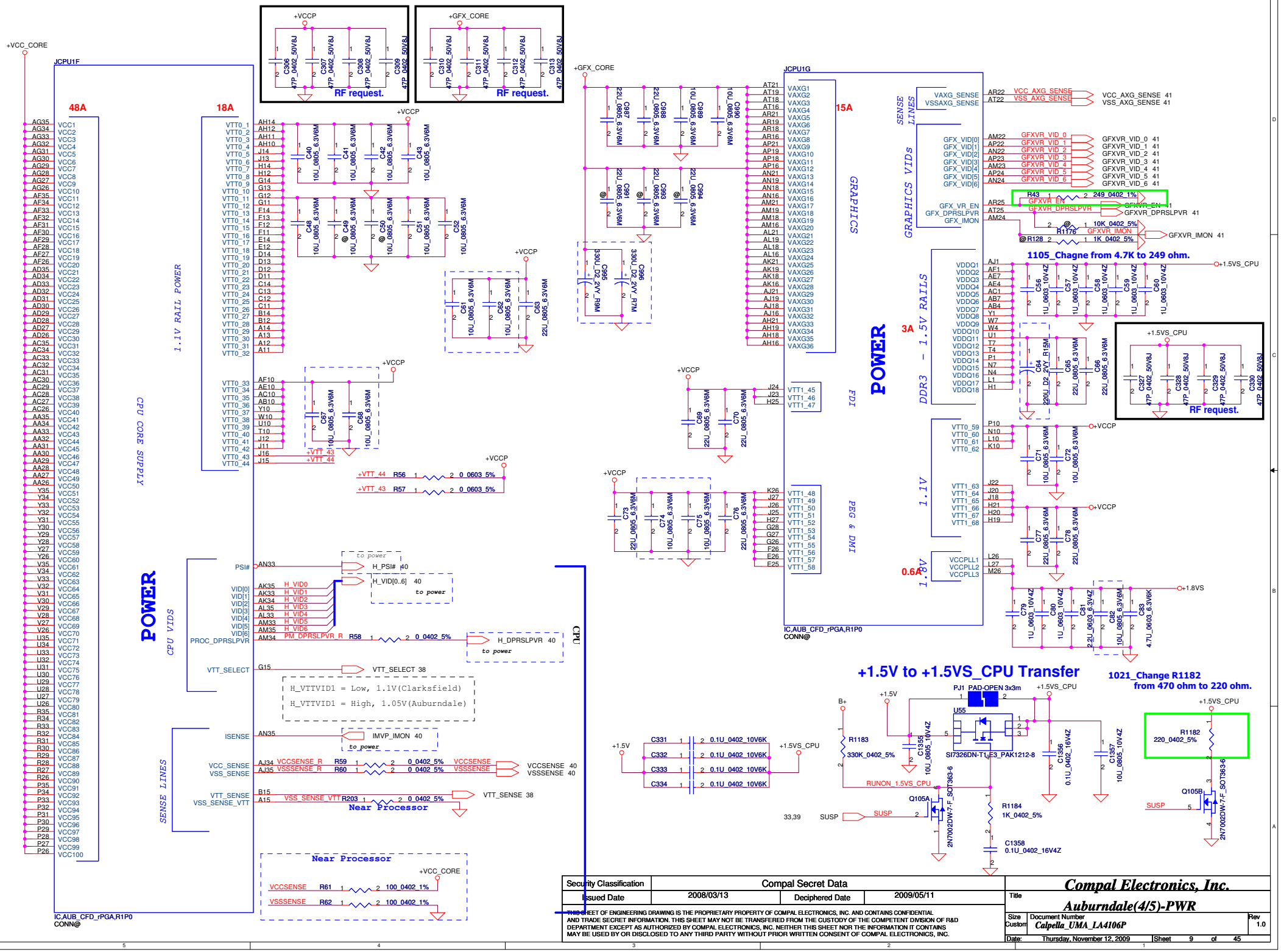


Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

Compal Electronics, Inc.			
Title: Cantiga(2/6)-DDR3 A/B CH			
Size: Custom	Document Number: Calpella_UMA_LA4106P		Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 8 of 45		



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Title	Auburndale(4/5)-PWR
Size: Custom	Document Number: Calpella_UMA_LA4106P
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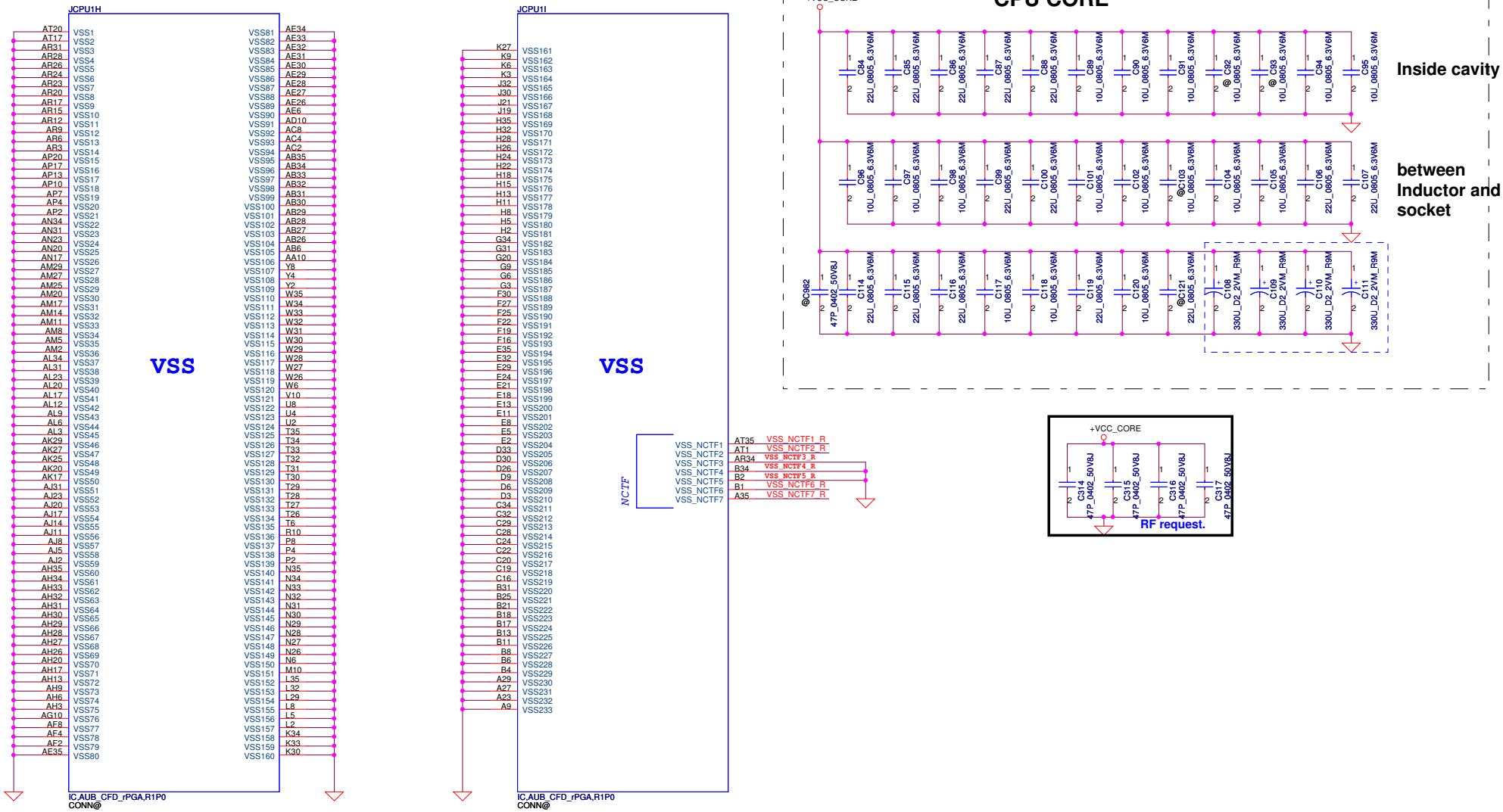
Date: Thursday, November 12, 2009	Sheet 9 of 45



Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

Compal Electronics, Inc.

Title: Auburndale(5/5)-GND/Bypass

Size	Document Number	Rev
Custom	Calpella_UMA_LA4106P	1.0

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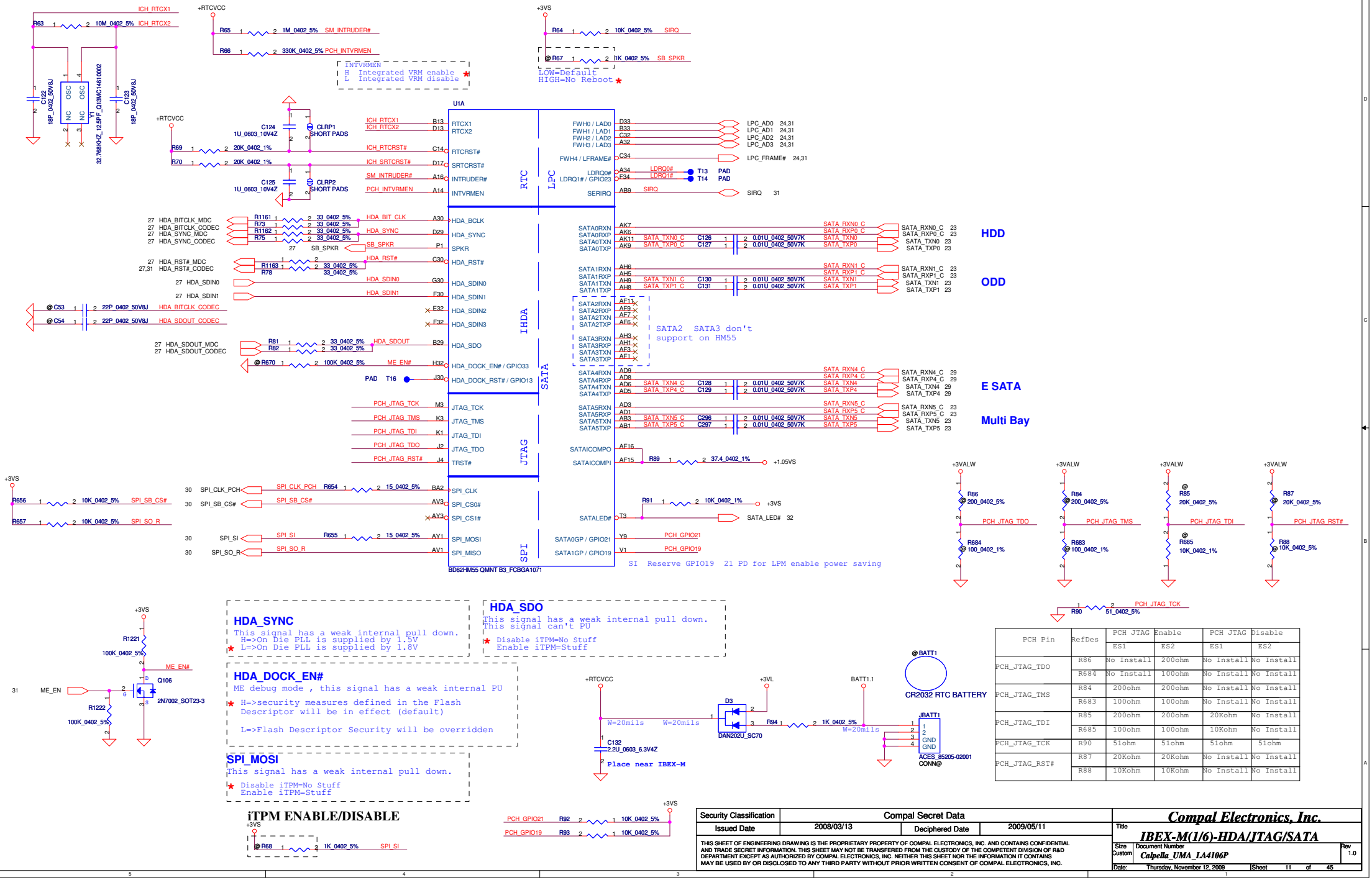

PCH Pin	RefDes	PCH JTAG Enable ES1	PCH JTAG Enable ES2	PCH JTAG Disable ES1	PCH JTAG Disable ES2
PCH_JTAG_TDO	R86	No Install	200ohm	No Install	No Install
	R684	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R84	200ohm	200ohm	No Install	No Install
	R683	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R85	200ohm	200ohm	20Kohm	No Install
	R685	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R90	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R87	20Kohm	20Kohm	No Install	No Install
	R88	10Kohm	10Kohm	No Install	No Install

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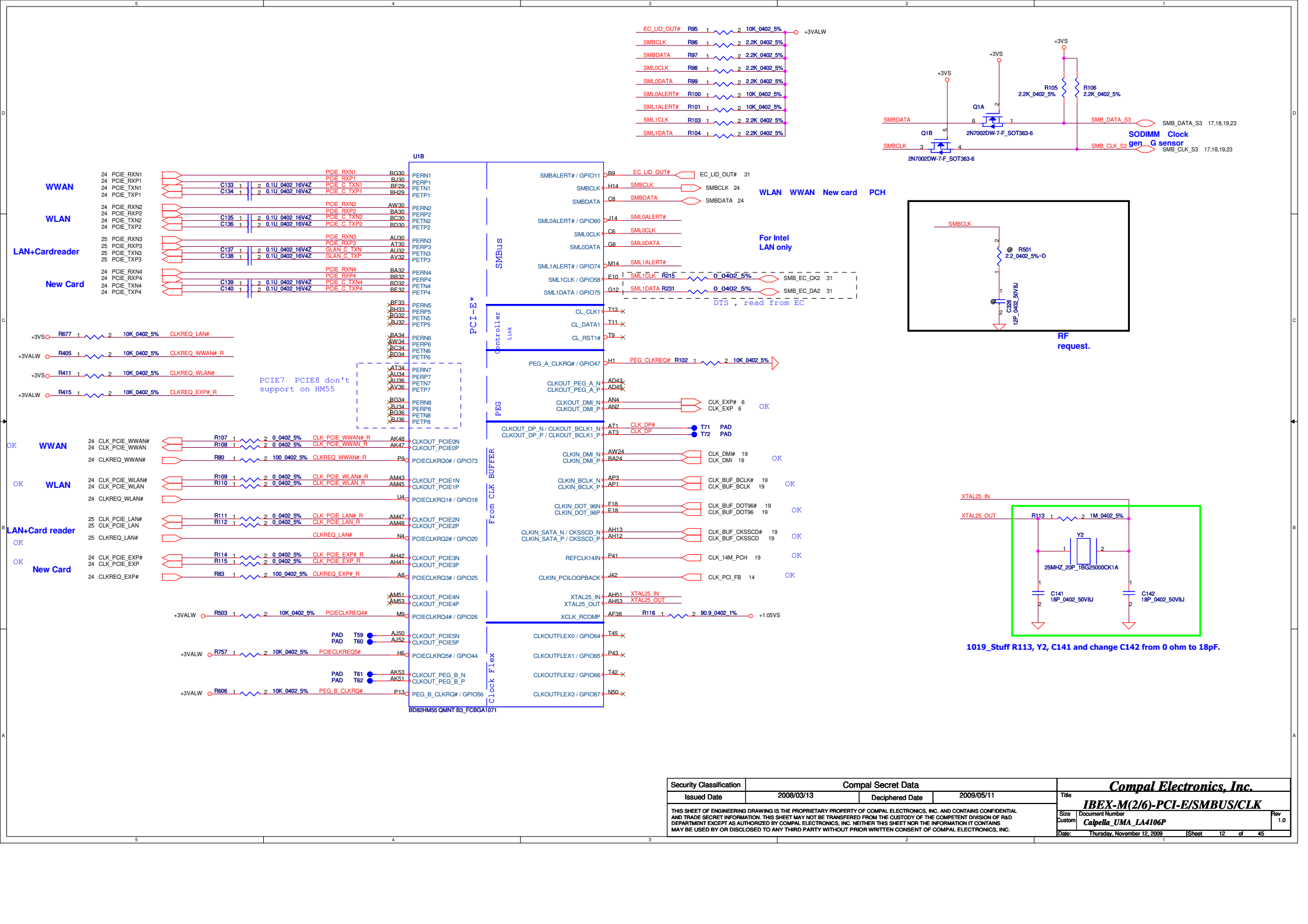
Issued Date	2008/03/13	Deciphered Date	2009/05/11

Compal Electronics, Inc.

Title: IBEX-M(1/6)-HDA/JTAG/SATA

Size: Custom | Document Number: Calpella_UMA_LA4106P | Rev: 1.0

Date: Thursday, November 12, 2009 | Sheet 11 of 45



Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

Compal Electronics, Inc.

Title: **IBEX-M(2/6)-PCI-E/SMBUS/CLK**

Size	Document Number	Rev
Custom	Calpella_UMA_LA4106P	1.0

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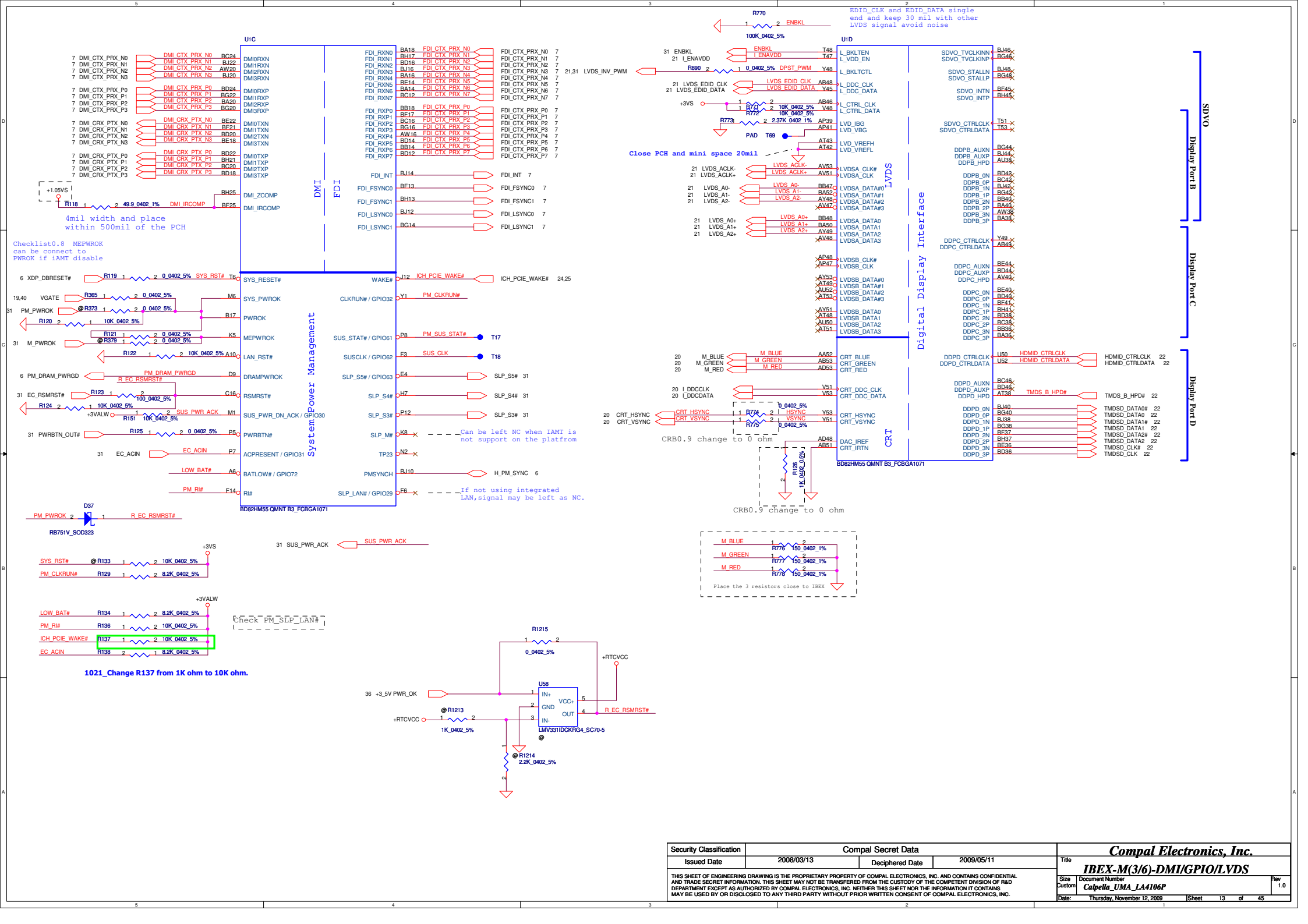

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Compal Electronics, Inc.

Title: **IBEX-M(3/6)-DMI/GPIO/LVDS**

Size	Document Number	Rev
Custom	Calpella_UMA_LA4106P	1.0

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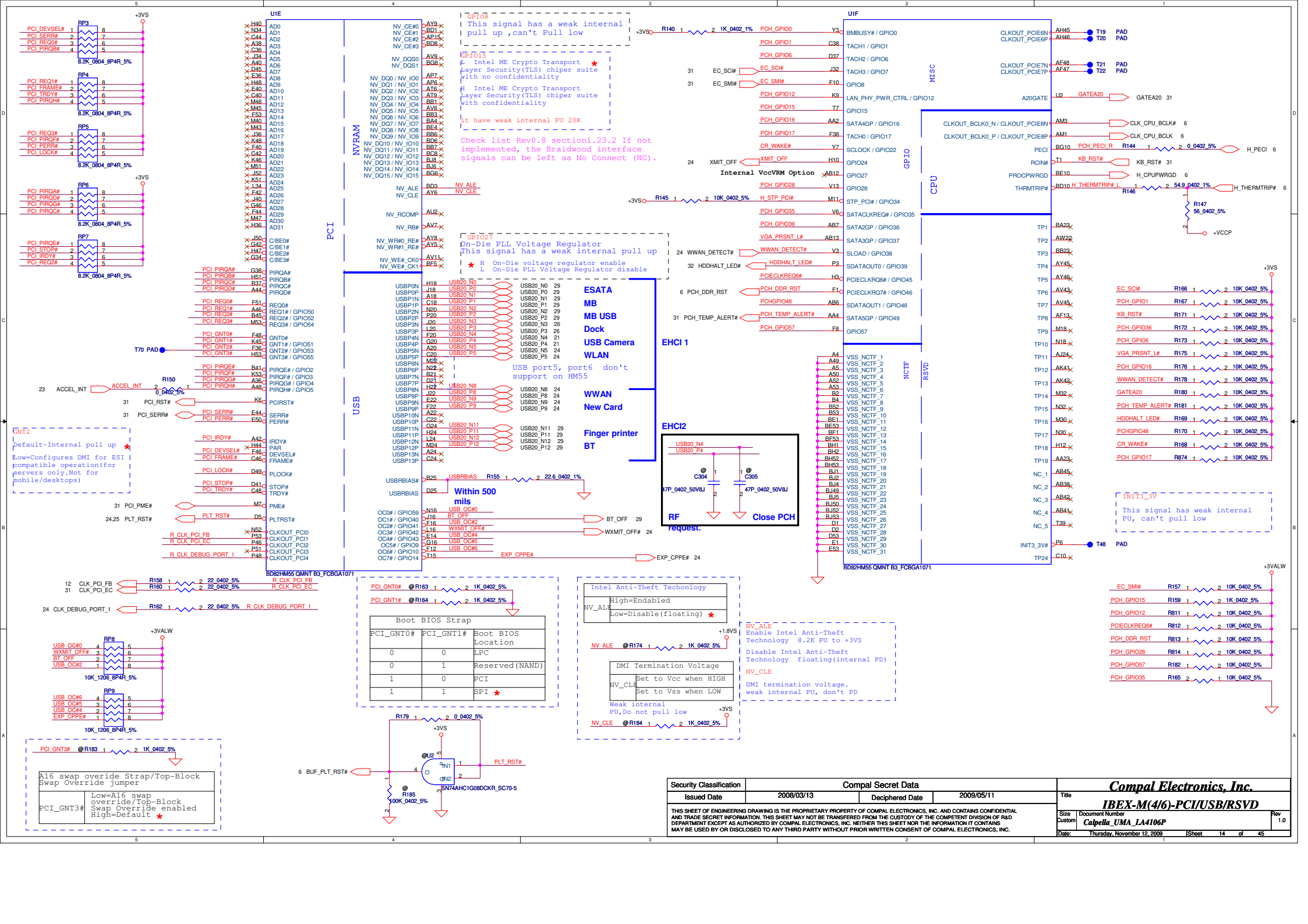
U1E
PCI
NVRAM
USB
U1F
CPU
GPIO
MISC
RSVD
NCTF
BD82HM55 QMNT B3_FCBGA1071
ESATA
MB
MB USB
Dock
USB Camera
WLAN
EHCI 1
USB port5, port6 don't support on HM55
WWAN
New Card
Finger printer
BT
EHCI2
RF
Close PCH
Request.
Within 500 mils
Internal VccVRM Option
GPIO8
This signal has a weak internal pull up ,can't Pull low
GPIO15
H Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality
H Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality
It have weak internal PU 20K
Check list Rev0.8 section1.23.2 If not implemented, the Braidwood interface signals can be left as No Connect (NC).
GPIO27
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
H On-Die voltage regulator enable
L On-Die PLL Voltage Regulator disable
GNT2
Default-Internal pull up
Low=Configures DMI for ESI compatible operation(for servers only.Not for mobile/desktops)
Boot BIOS Strap
PCI_GNT0#
PCI_GNT1#
Boot BIOS Location
0 0 LPC
0 1 Reserved(NAND)
1 0 PCI
1 1 SPI
Intel Anti-Theft Techonlogy
NV_ALE
High=Endabled
Low=Disable(floating)
DMI Termination Voltage
NV_CLE
Set to Vcc when HIGH
Set to Vss when LOW
Weak internal PU,Do not pull low
NV_ALE
Enable Intel Anti-Theft Technology 8.2K PU to +3VS
Disable Intel Anti-Theft Technology floating(internal PD)
NV_CLE
DMI termination voltage. weak internal PU, don't PD
A16 swap overide Strap/Top-Block Swap Override jumper
PCI_GNT3#
Low=A16 swap override/Top-Block Swap Override enabled
High=Default
INIT3_3V
This signal has weak internal PU, can't pull low
SN74AHC1G08DCKR_SC70-5
Security Classification
Compal Secret Data
Issued Date
2008/03/13
Deciphered Date
2009/05/11
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Title
IBEX-M(4/6)-PCI/USB/RSVD
Size Custom
Document Number
Calpella_UMA_LA4106P
Rev 1.0
Date: Thursday, November 12, 2009
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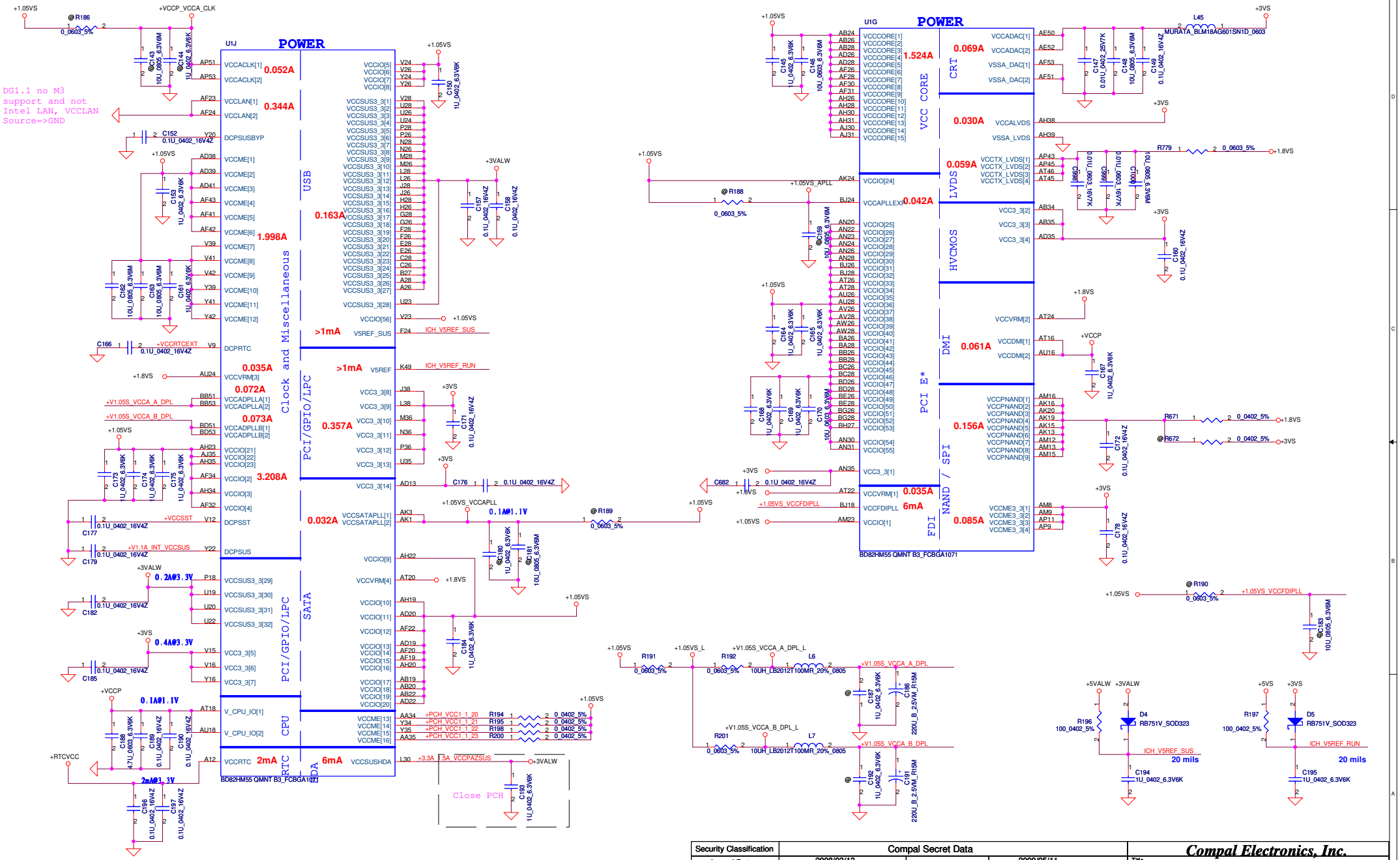

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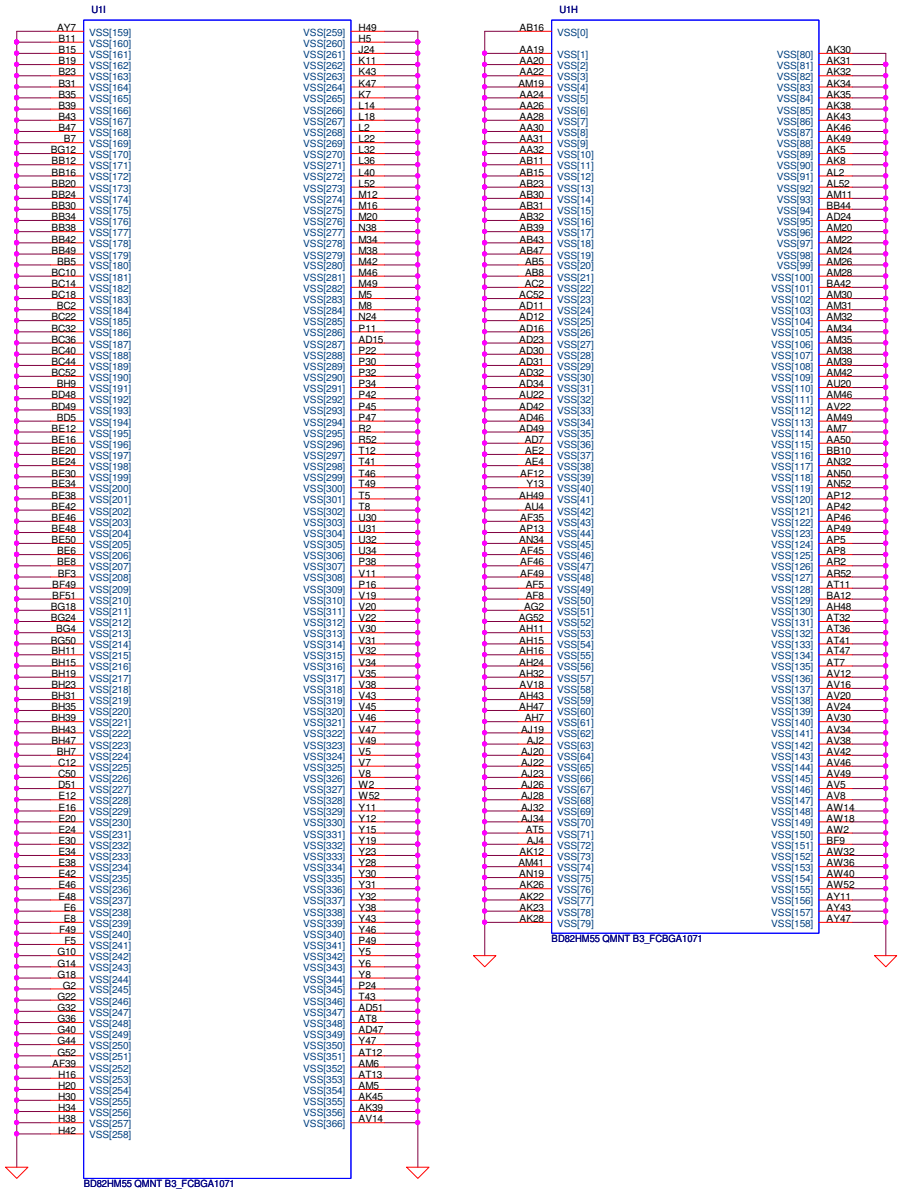
Issued Date	2008/03/13	Deciphered Date	2009/05/11

Compal Electronics, Inc.

Title: **IBEX-M(5/6)-PWR**

Size	Document Number	Rev
Custom	Calpella_UMA_LA4106P	1.0

Date: Thursday, November 12, 2009 | Sheet 15 of 45



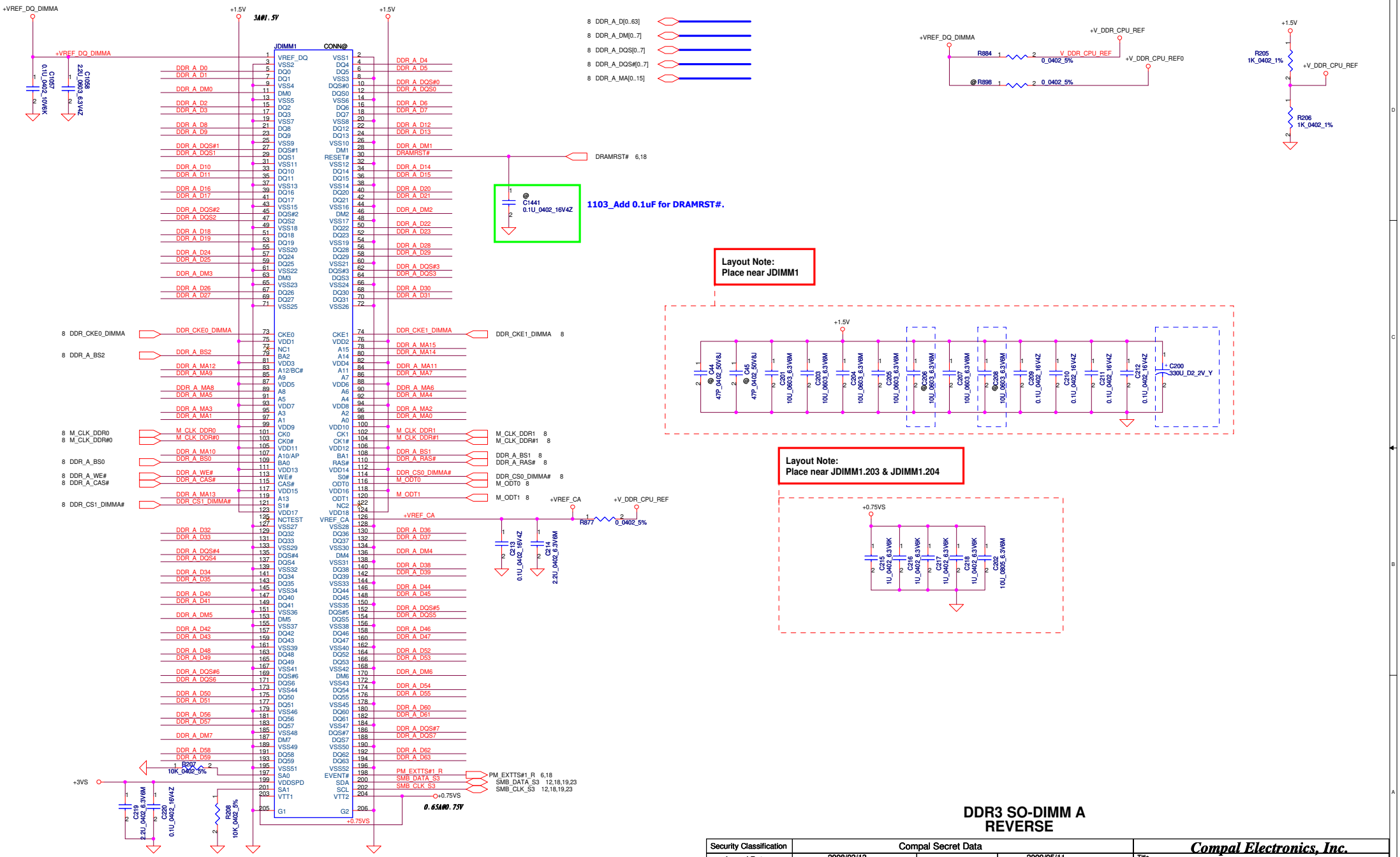
Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

Compal Electronics, Inc.

Title: **IBEX-M(6/6)-GND**

Size	Document Number	Rev
Custom	Calpella_UMA_LA4106P	1.0

Date: Thursday, November 12, 2009 | Sheet 16 of 45



DDR3 SO-DIMM A REVERSE

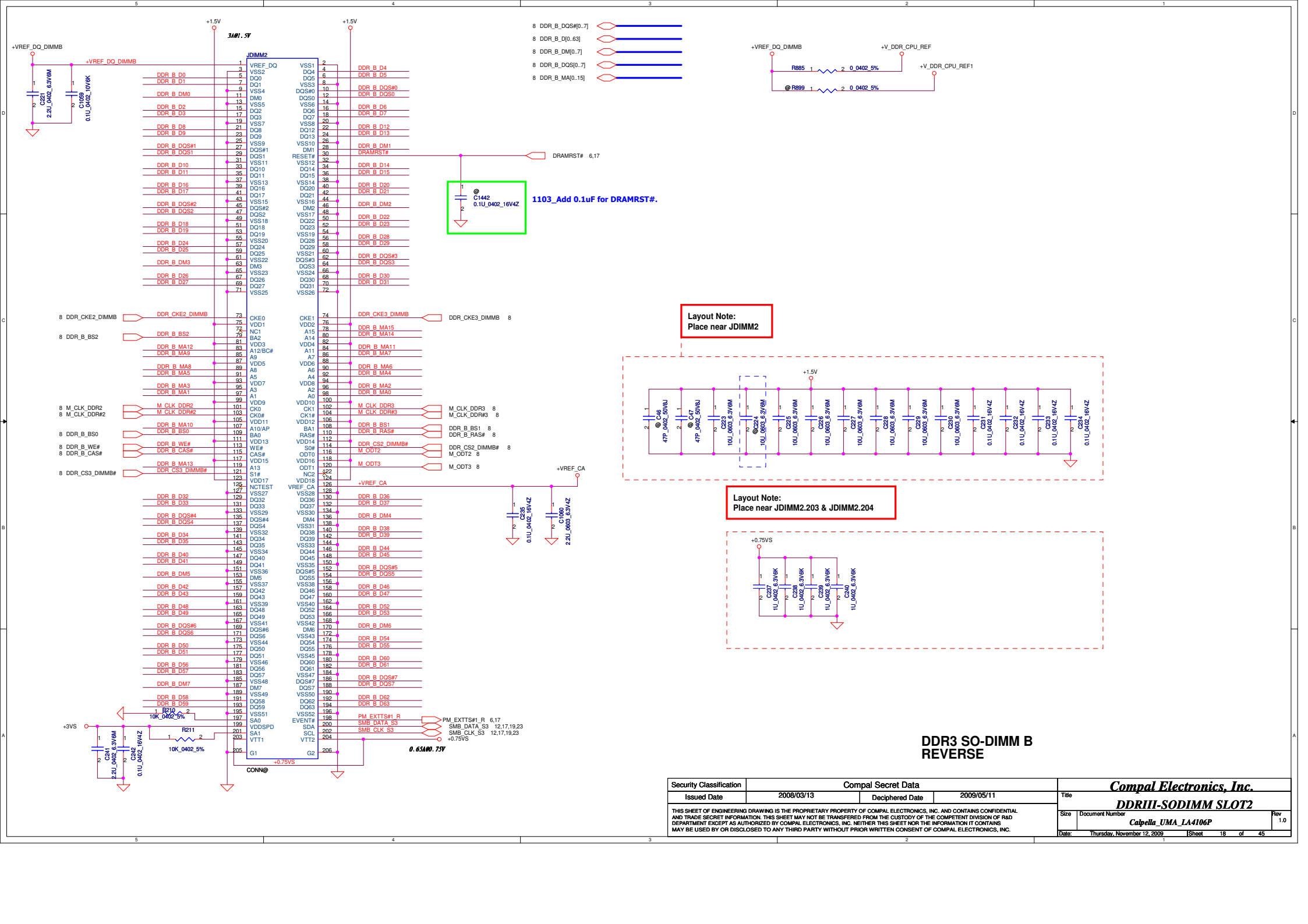
Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size	Document Number	Rev
Custom	Calpella_UMA_LA4106P	1.0

Date: Thursday, November 12, 2009 | Sheet 17 of 45



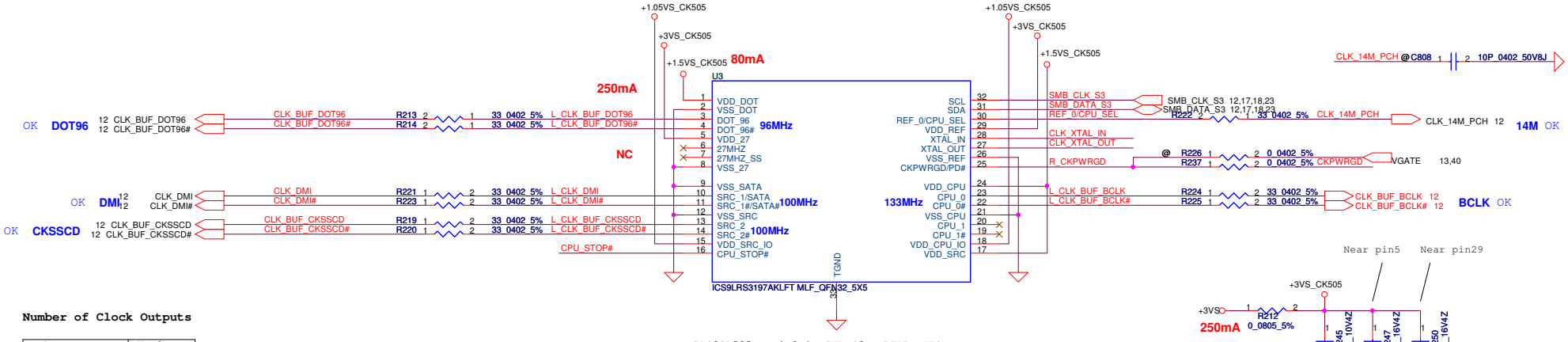
Security Classification	Compal Secret Data		
Issued Date	2008/03/13	Deciphered Date	2009/05/11

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size	Document Number	Rev
	Calpella_UMA_LA4106P	1.0

Date: Thursday, November 12, 2009 | Sheet 18 of 45



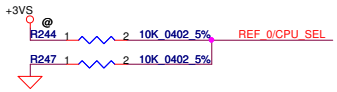
SLG8SP585 pin8 is GND (for DELL HP)
SLG8SP587 pin8 is 48MHz (For ABO or 030)

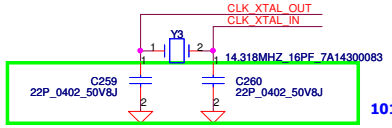
Number of Clock Outputs

Output	Number
133MHz	2
SRC(100MHz_SS)	1
SRC/SATA(100MHz)	1
REF(14.318MHz)	1
DOT_CLK(96MHz)	1
27MHz	1
27MHz_SS	1

PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1	100MHz	100MHz

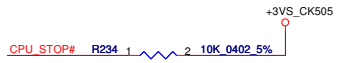
CPU_SEL During CK_PEWGD Latch Pin1

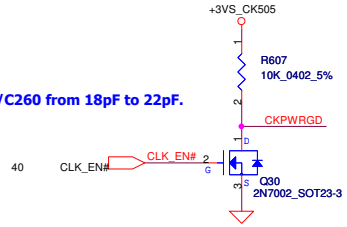




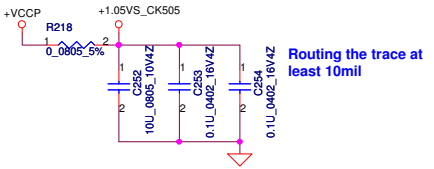
Vendor suggests 22pF

1019_Change C259/C260 from 18pF to 22pF.

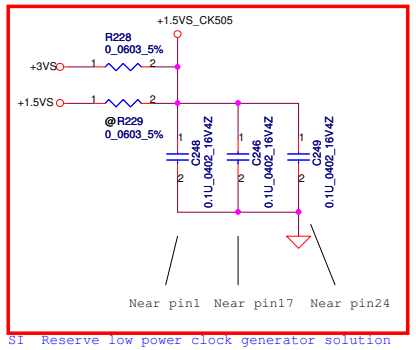




Place close to U3



Routing the trace at least 10mil



SI Reserve low power clock generator solution

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

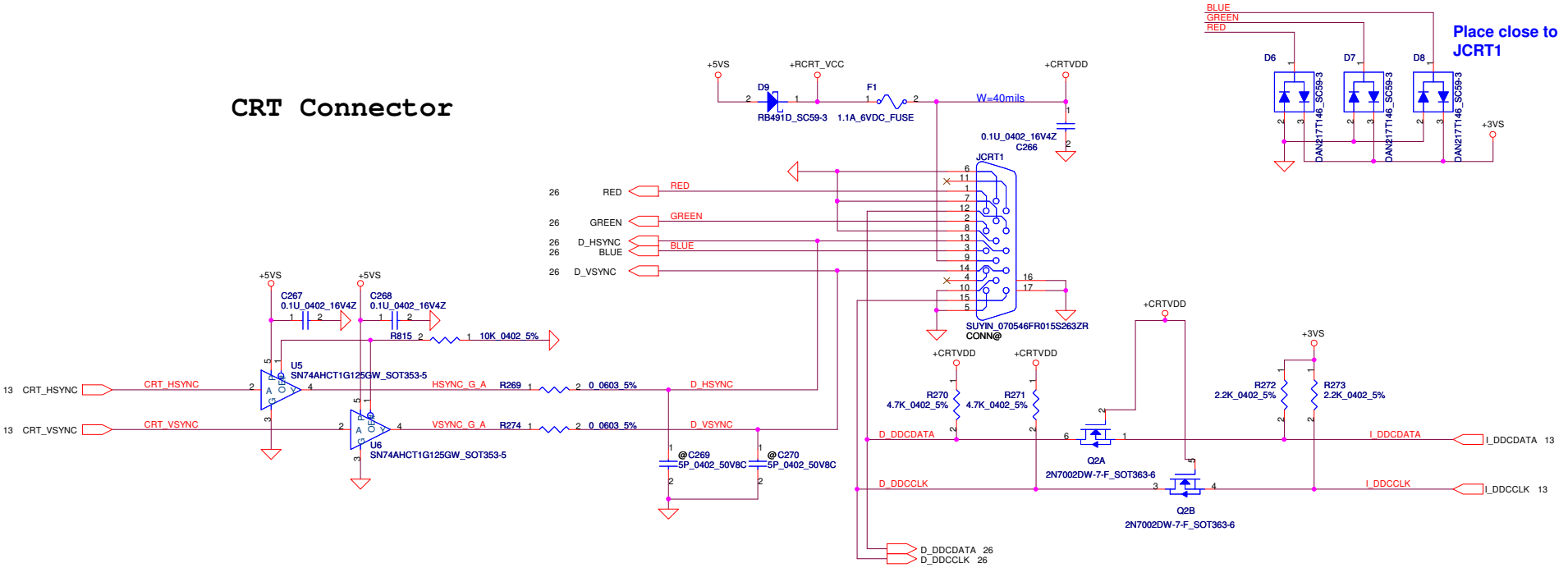
Compal Electronics, Inc.

Title: **Clock Generator CK505**

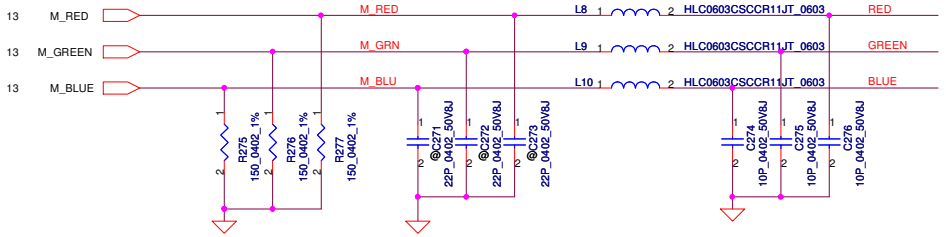
Size	Document Number	Rev
	Calpella_UMA_LA4106P	1.0

Date: Thursday, November 12, 2009 Sheet 19 of 45

CRT Connector



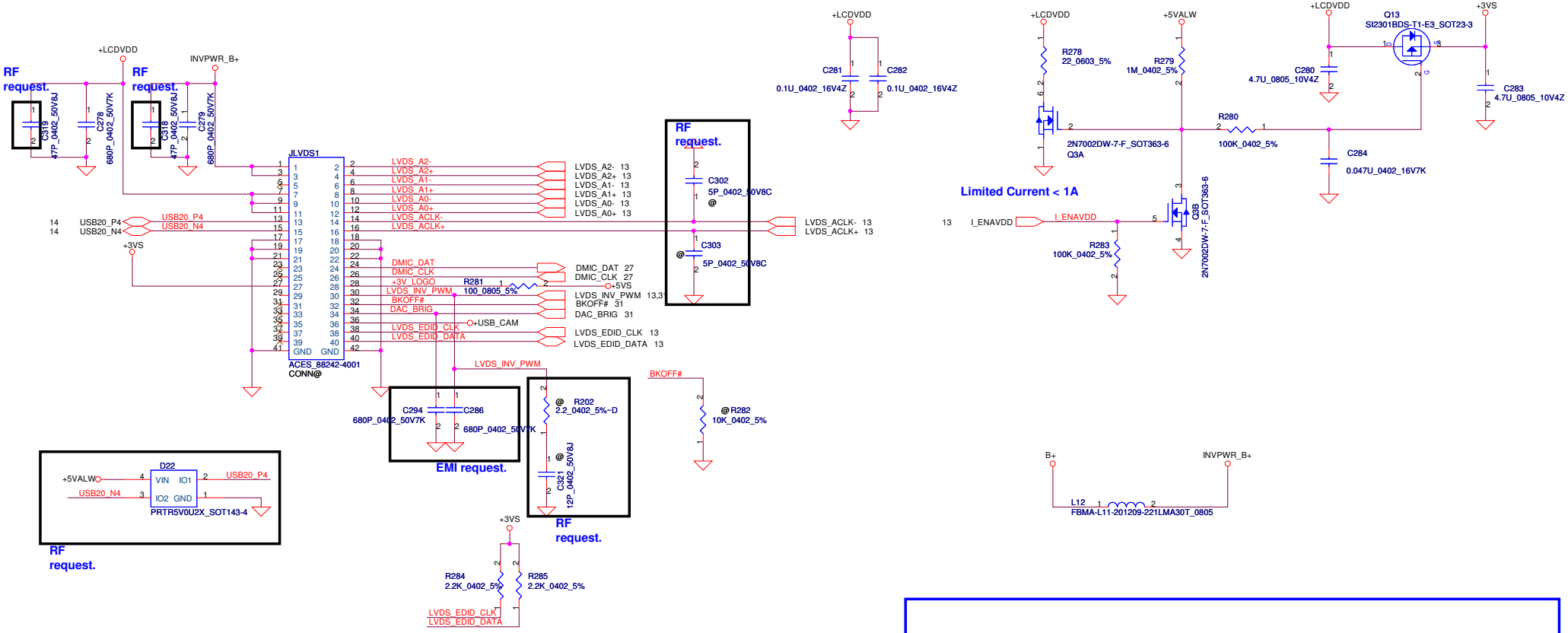
CRT Termination/EMI Filter

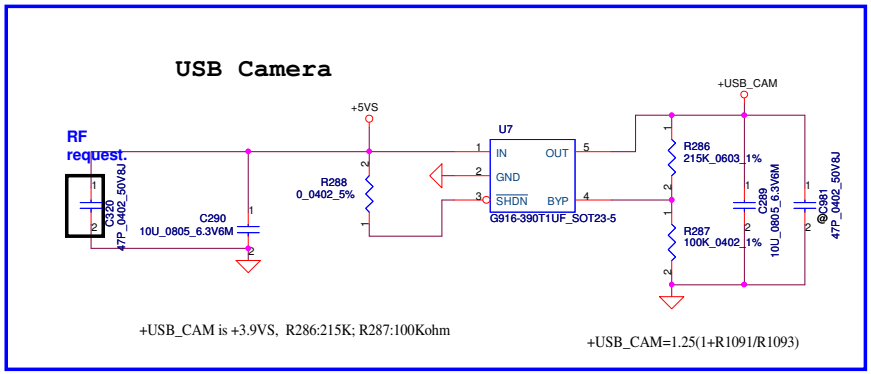


Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: CRT Connector			
Size	Document Number: Calpella_UMA_LA4106P		Rev: 1.0
Date: Thursday, November 12, 2009		Sheet 20 of 45	

LVDS CONN & USB Camera + Dig Mic



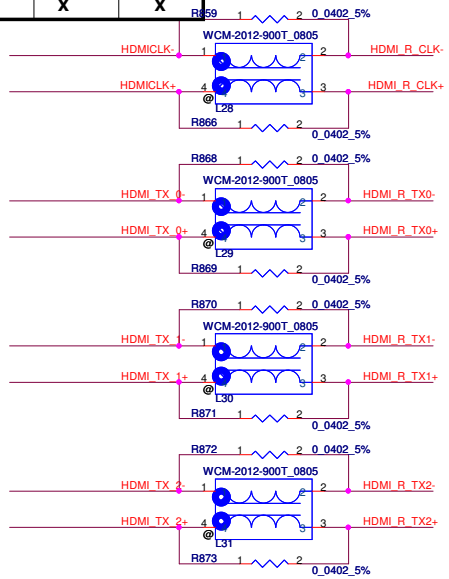


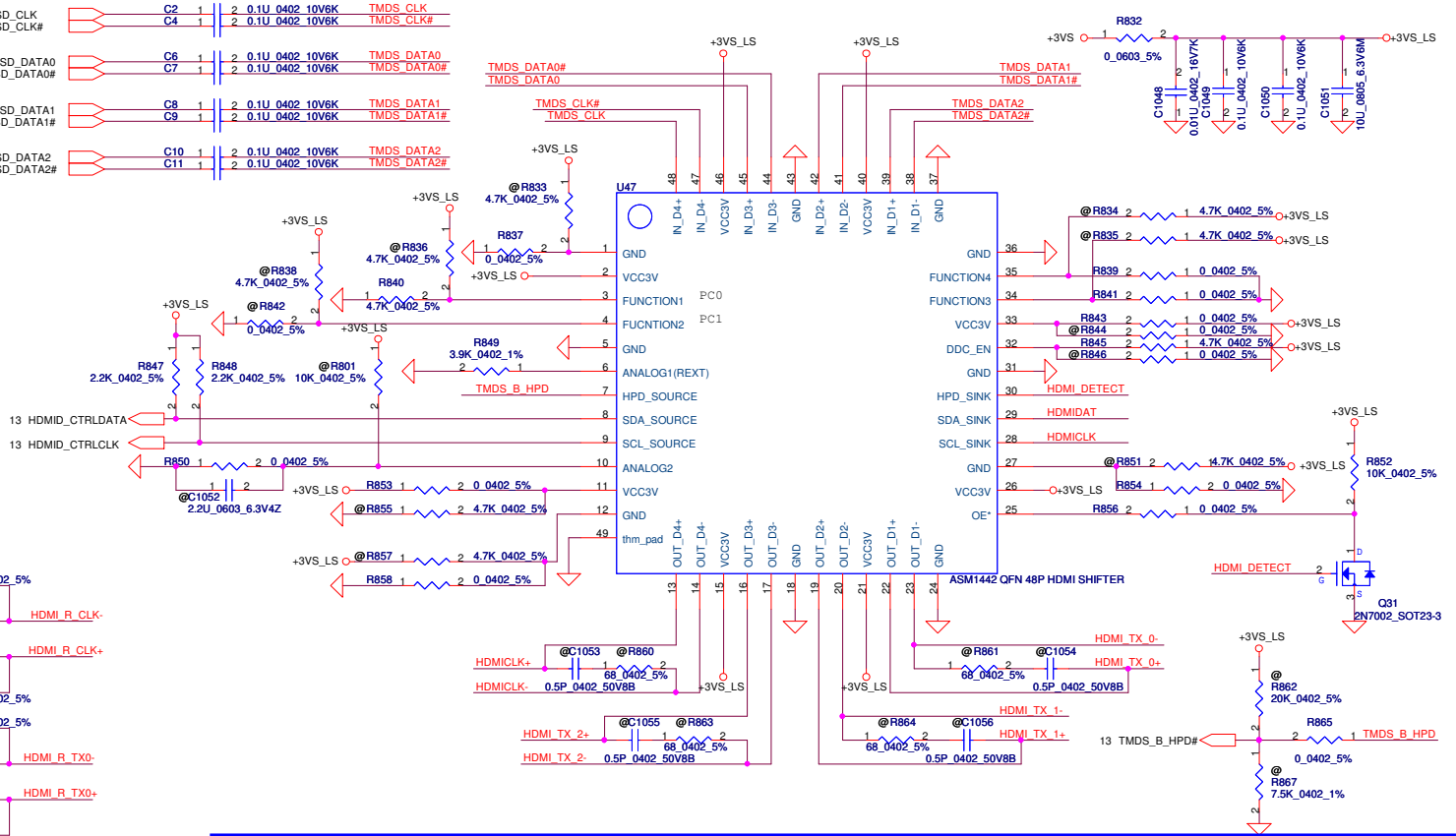
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

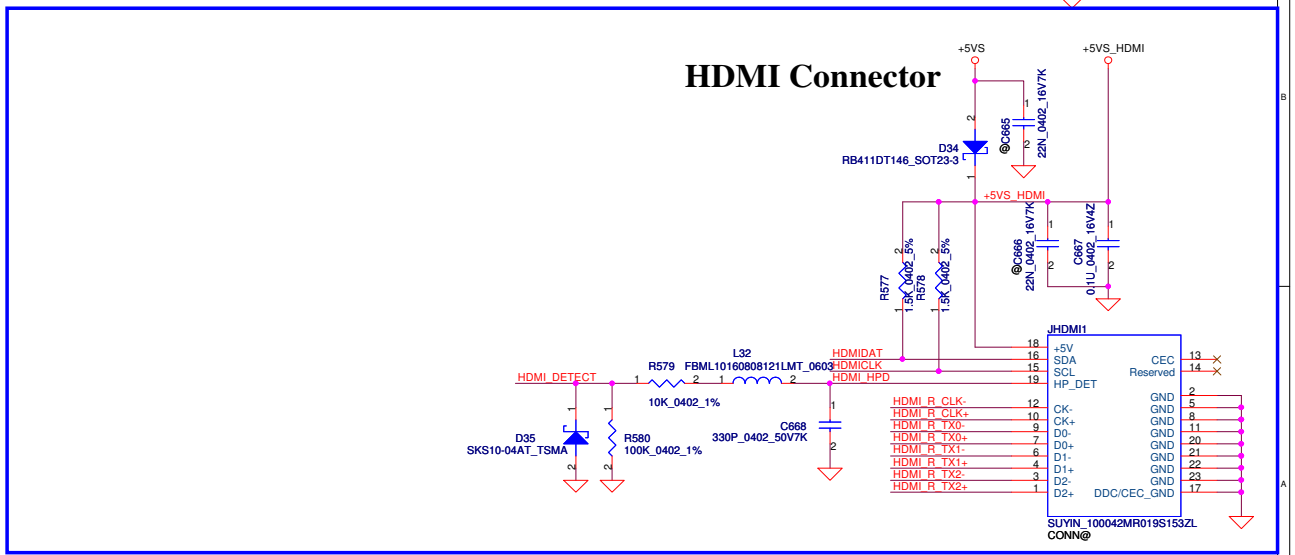
Compal Electronics, Inc.			
Title	LCD CONN.		
Size	Document Number	Rev	
	Calpella_UMA_LA4106P	1.0	
Date: Thursday, November 12, 2009	Sheet 21 of 45		

	ST	Parade 8101T	8171	Asmedia 1442	TI
R833	X	X	X	X	X
R837	0 ohm	0 ohm	4.7K ohm	0 ohm	0 ohm
R836	X	4.7K ohm	X	X	4.7K ohm
R840	4.7K ohm	X	4.7K ohm	4.7K ohm	X
R838	X	X	4.7K ohm	X	4.7K ohm
R842	X	X	X	X	X
R849	3.9K ohm	499 ohm	499 ohm	3.9K ohm	4.3K ohm
R850	0 ohm	X	X	0 ohm	X
C1052	X	X	2.2uF	X	X
R853	0 ohm	0 ohm	X	0 ohm	0 ohm
R855	X	X	4.7K ohm	X	X
R857	X	X	4.7K ohm	X	X
R858	0 ohm	0 ohm	X	0 ohm	0 ohm
R851	X	X	4.7K ohm	X	X
R854	0 ohm	0 ohm	X	0 ohm	0 ohm
R843	0 ohm	0 ohm	X	0 ohm	0 ohm
R844	X	X	4.7K ohm	X	X
R839	0 ohm	X	4.7K ohm	0 ohm	0 ohm
R834	X	X	X	X	X
R841	0 ohm	X	X	0 ohm	0 ohm
R835	X	X	4.7K ohm	X	X
C667	0.1uF	1uF	1uF	0.1uF	1uF
R862	V	X	X	X	X
R867	V	X	X	X	X

EQUALIZATION SETTING:
[PC1,PC0]=00,8dB
[PC1,PC0]=01,4dB (Recommanded)
[PC1,PC0]=10,12dB
[PC1,PC0]=11,0dB



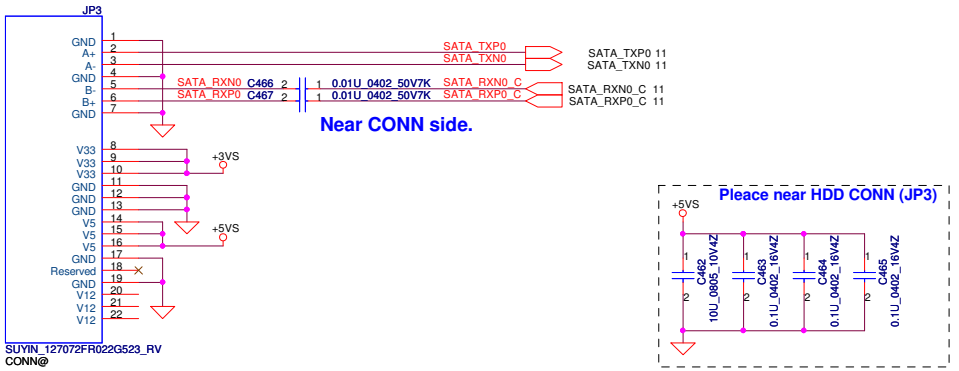




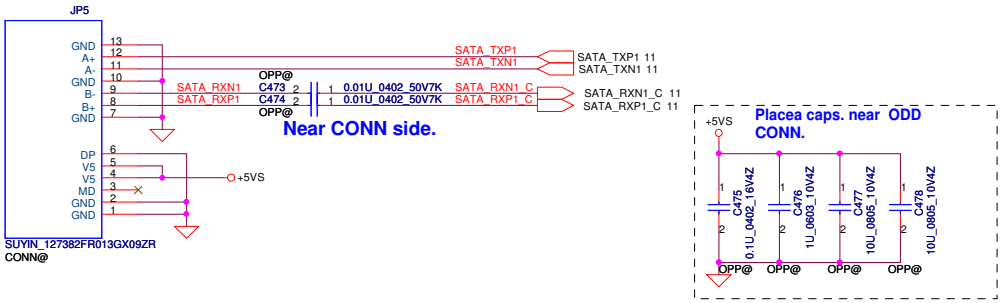
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.	
Title	HDMI LS & Conn.
Size: Custom	Document Number: Calpella_UMA_LA4106P
Rev	1.0
Date: Thursday, November 12, 2009	Sheet 22 of 45

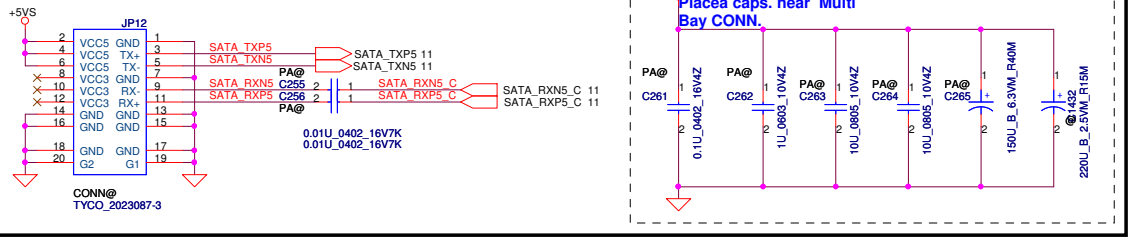
HDD Connector



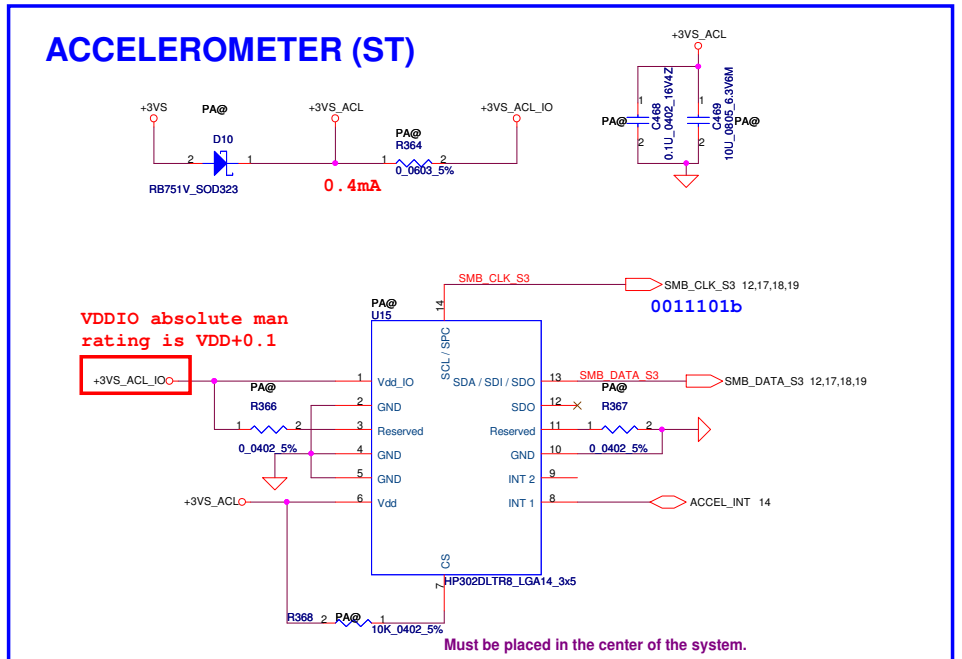
CD-ROM Connector



Multi Bay



ACCELEROMETER (ST)



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.

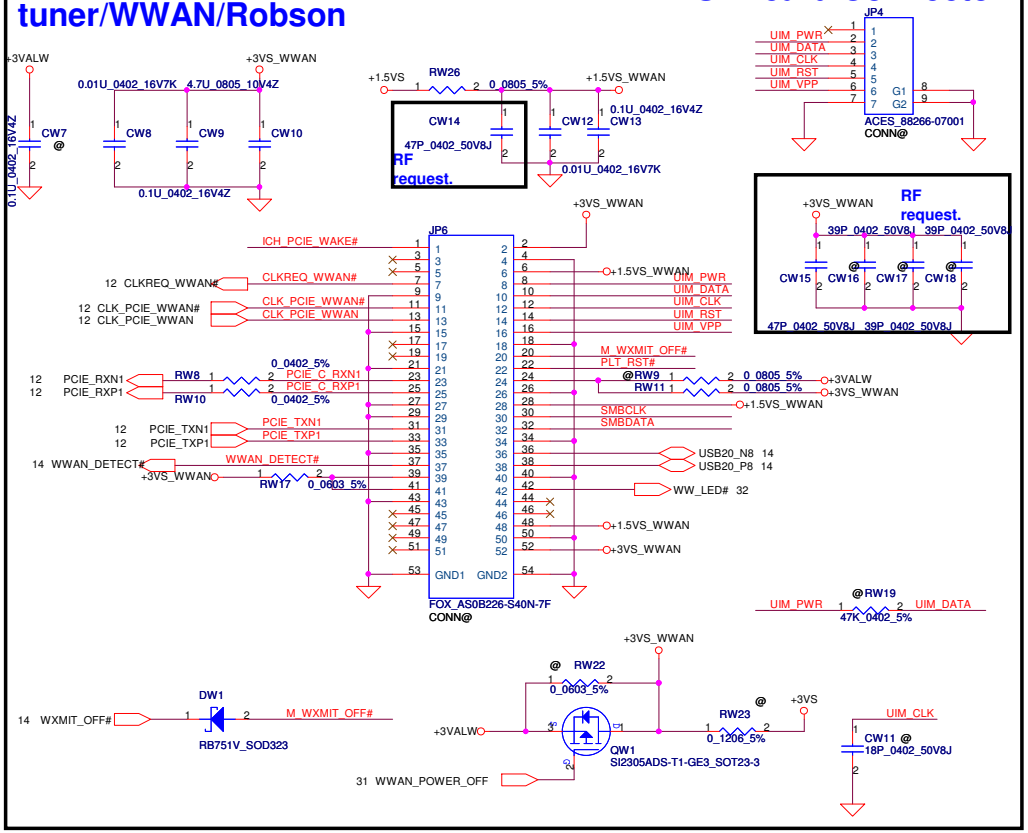
Title: HDD & CDROM

Size	Document Number	Rev
Custom	Calpella_UMA_LA4106P	1.0

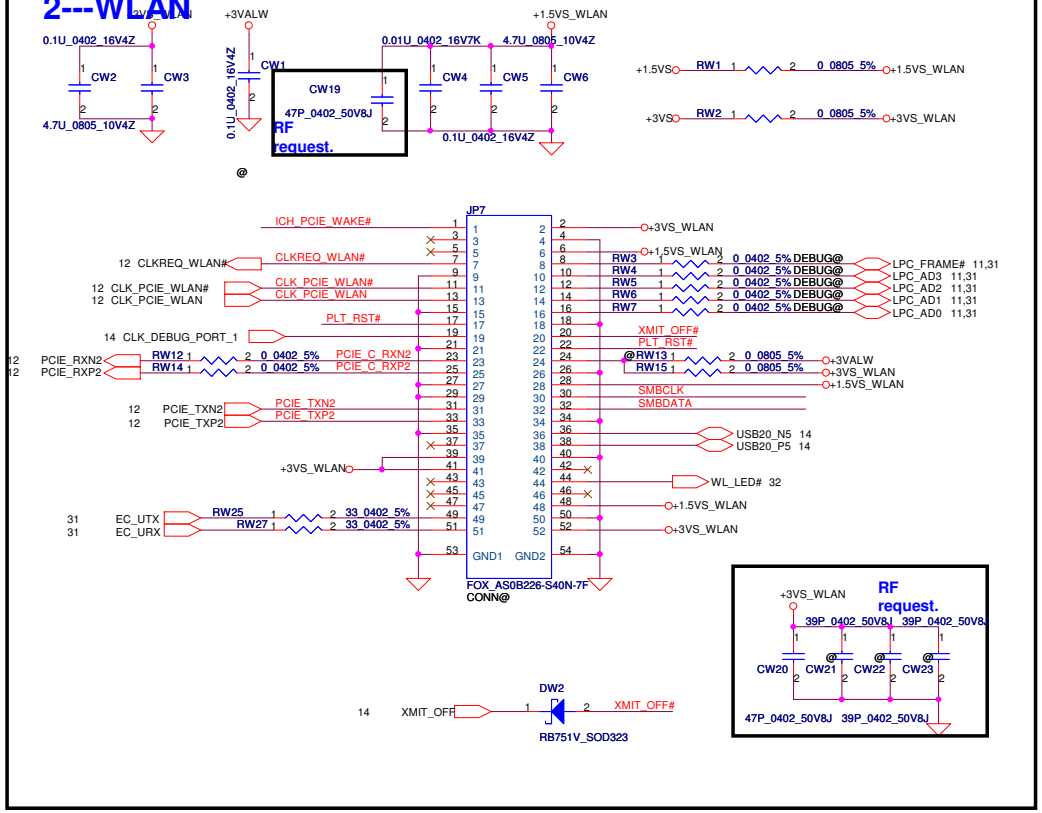
Date: Thursday, November 12, 2009 | Sheet 23 of 45

Mini Card 0--TV tuner/WWAN/Robson

SIM card Connector

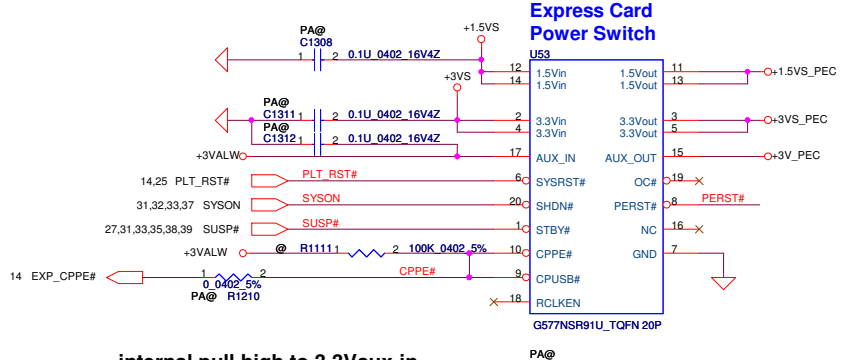


Mini Card 2---WLAN



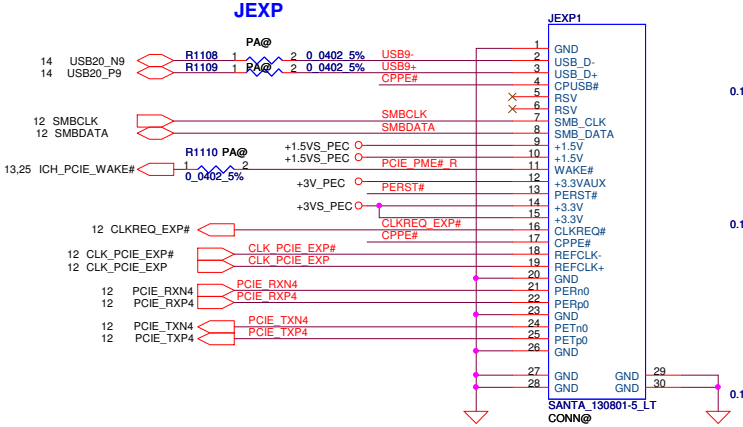
New Card

Express Card Power Switch

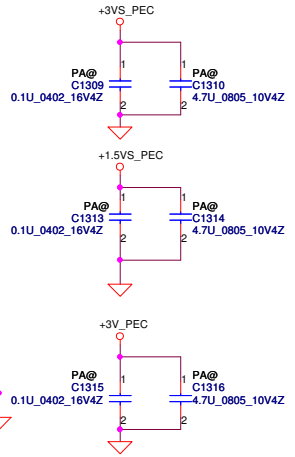


internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

Close to JEXP



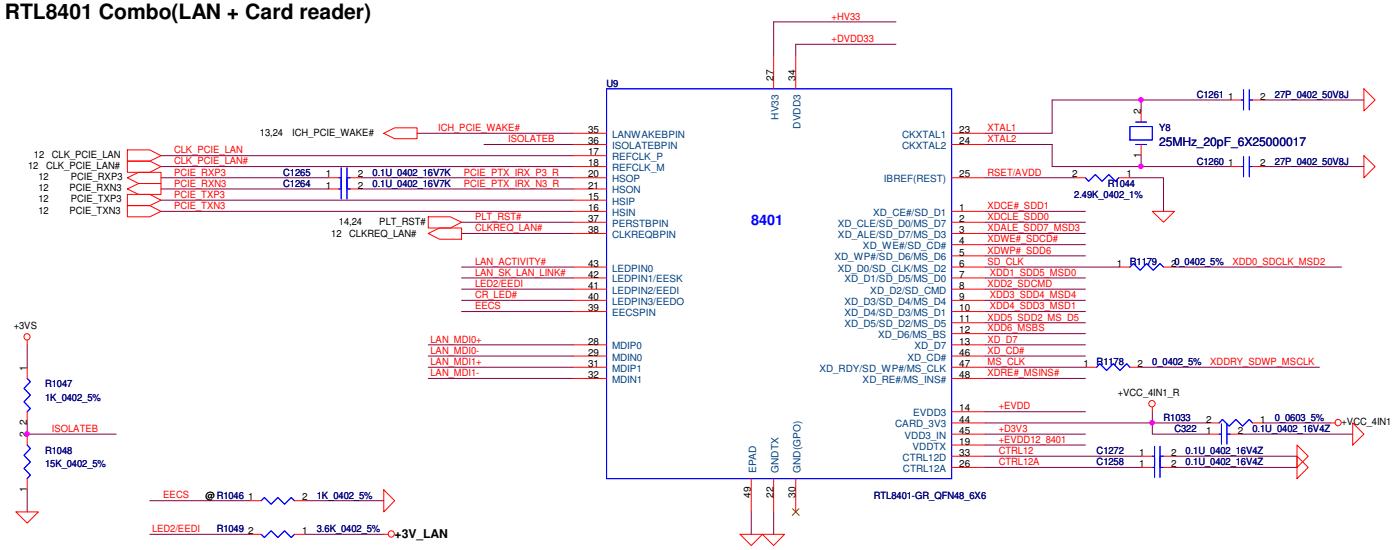
Near to Express Card slot.



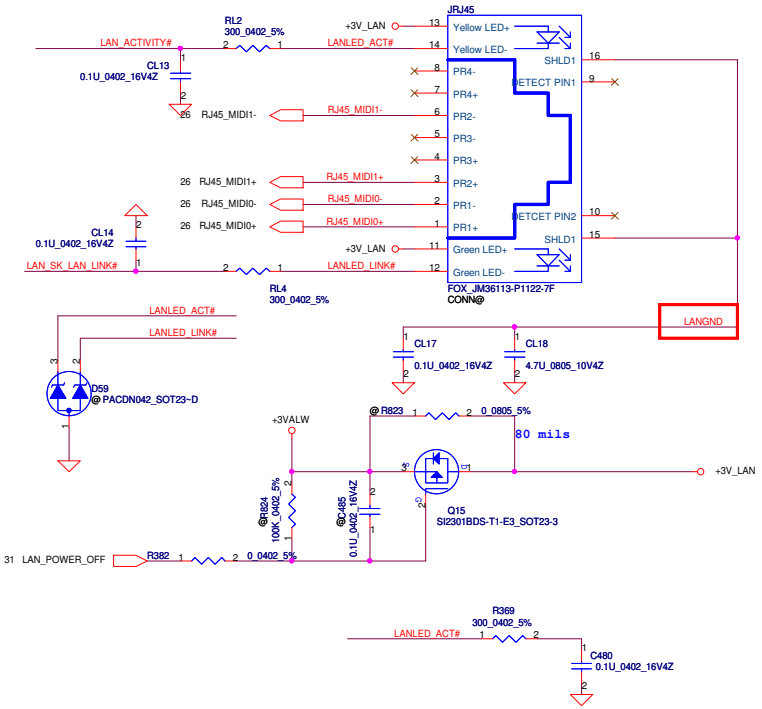
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.	
Title	WLAN, WWAN, New Card
Size	Document Number: Calpella_UMA_LA4106P
Rev	1.0
Date:	Thursday, November 12, 2009
Sheet	24 of 45

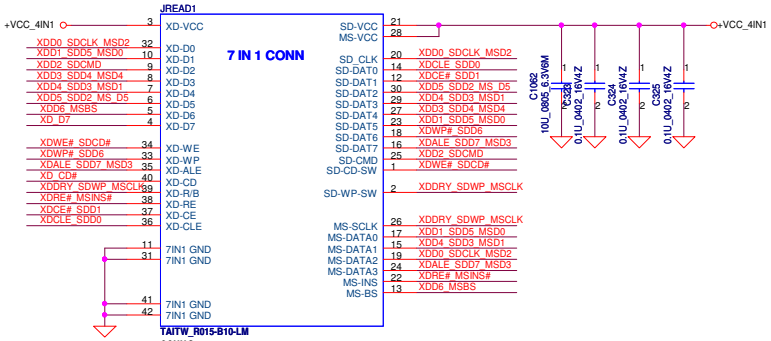
RTL8401 Combo(LAN + Card reader)



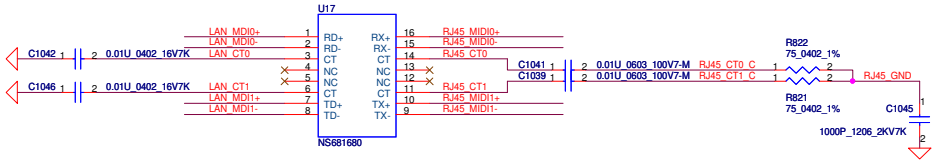
LAN Conn.



Card Reader Connector



10/100 Transformer



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/10/06

Compal Electronics, Inc.

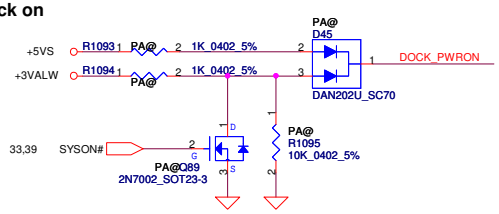
Title: **USB CardReader&CONN**

Size	Document Number	Rev
Custom	Calpella_UMA_LA4106P	1.0

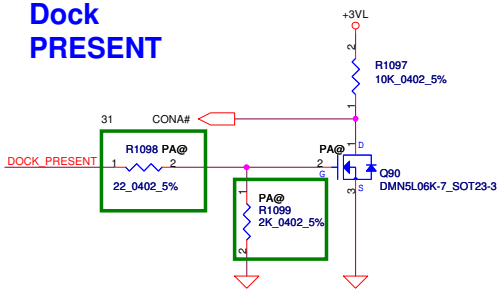
Date: Thursday, November 12, 2009 | Sheet 25 of 45

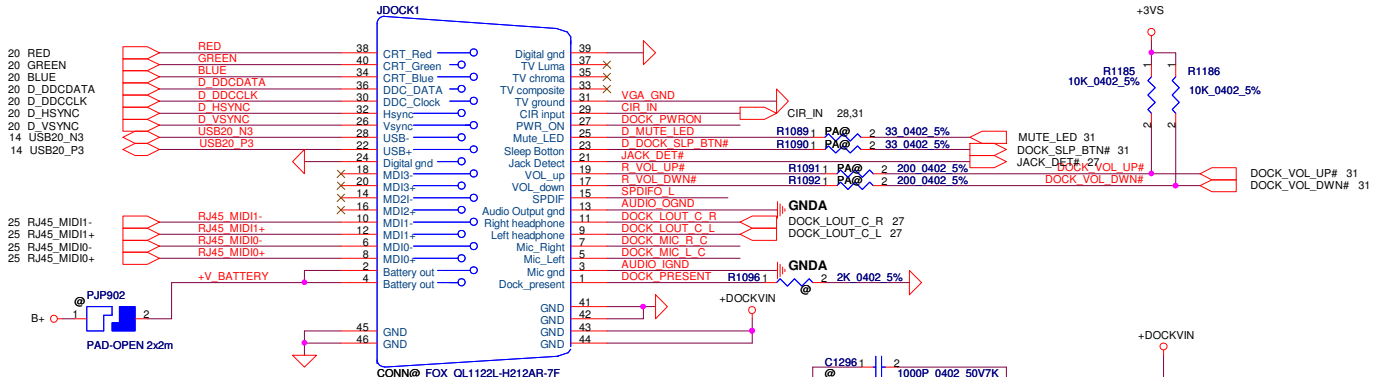
Atlas/ Saturn Dock

DOCK_PWR_ON Spec
0V = Notebook S4/S5,
Dock off
2.5V = Notebook S3,
Dock on
4V = Notebook S0,
Dock on

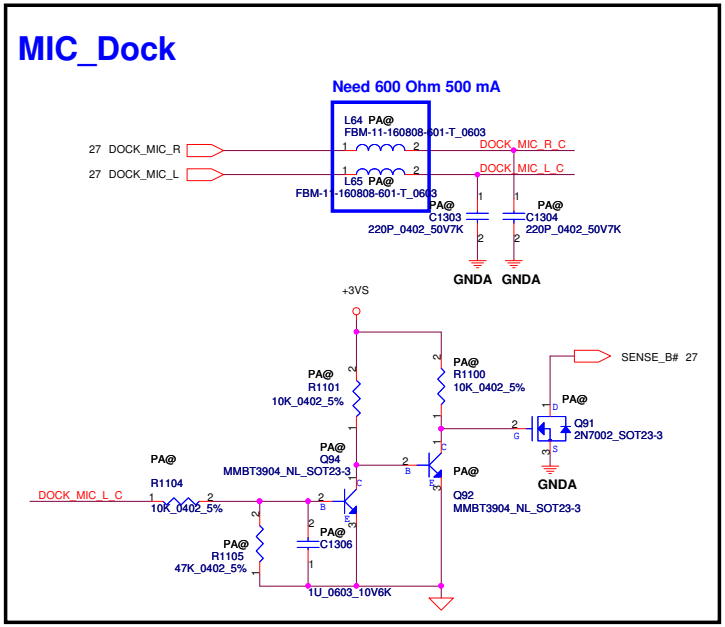


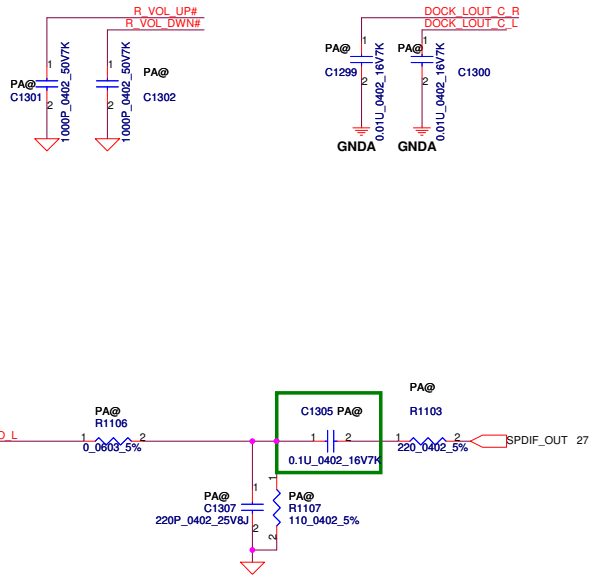
Dock PRESENT





MIC_Dock





Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.			
Title: DOCK CONN.			
Size: Custom	Document Number: Calpella_UMA_LA4106P		Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 26 of 45		

1105_Reserve the others +5VS power for Codec.

1102_Reserve LDO power for Codec.

1102_Reserve 4.7uF.

1105_Reserve 1230.

U22

92HD80B1X5NLGXYD38_QFN48_7X7~D

92HD80 port define	
Port A	DOCK HP
Port B	HP
Port C	INT. MIC
Port D	SPKR
Port E	DOCK MIC
Port F	EXT. MIC
DM0	Digital MIC

Dock HP Jack

HP Jack

Int. MIC

Internal SPKR

DOCK_MIC

Ext MIC

1/10*Vin need close to Codec

92HD80 Resistor define		
Resistor	SENSE_A	SENSE_B
39.2K	Port A HP1	Port E
20.2K	Port B	Port F
10.0K	Port C	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1
2.49K	PU to AVDD	PU to AVDD

CODEC POWER

(4.75V)
300mA

1102_Reserve CODEC LDO for Codec.

MDC 1.5 Conn.

JP8

ACES_88018-124G

CONN@

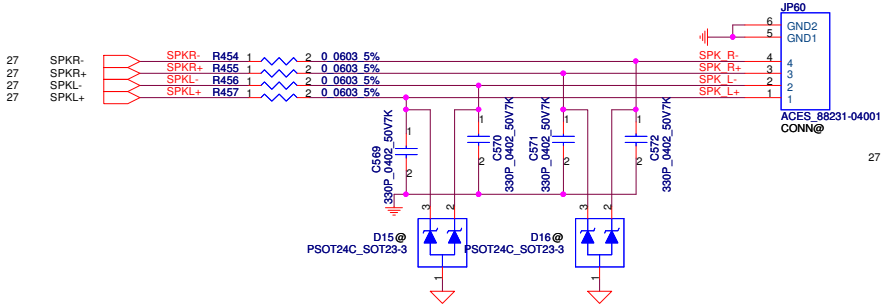
Connector for MDC Rev1.5

MDC Standoff

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

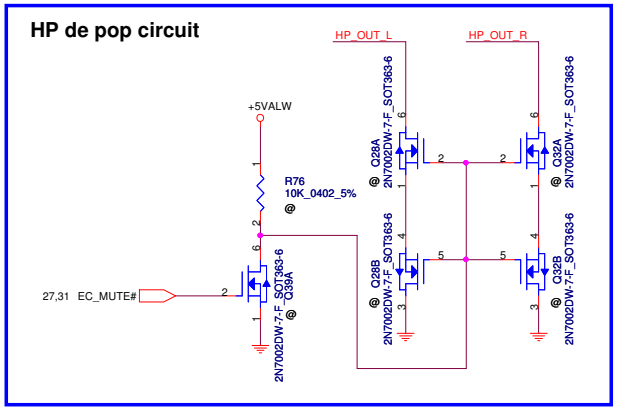
Title	Codec_IDT92HD80		
Size: Custom	Document Number: Calpella_UMA_LA4106P		Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 27 of 45		

SPEAKER

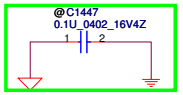


Audio connector

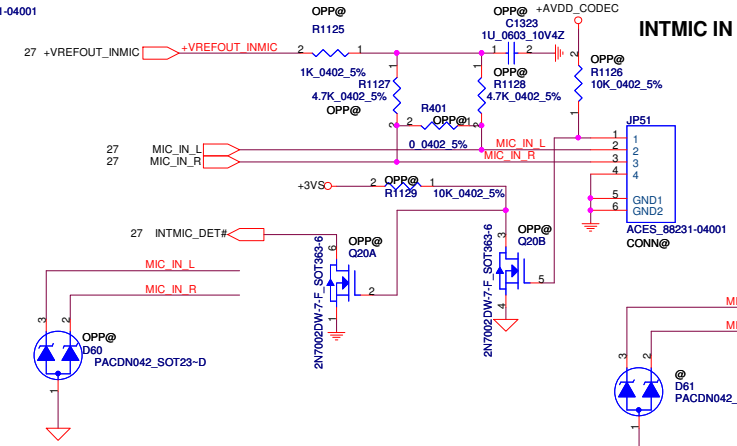
HP de pop circuit

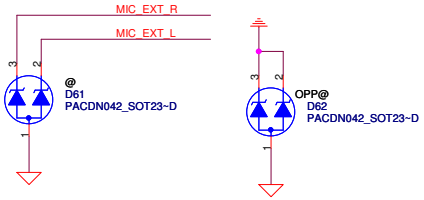


1103_Reserve 0.1uF between GND and GNDA.

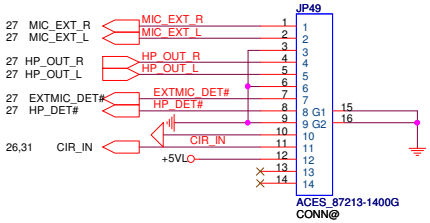


INTMIC IN





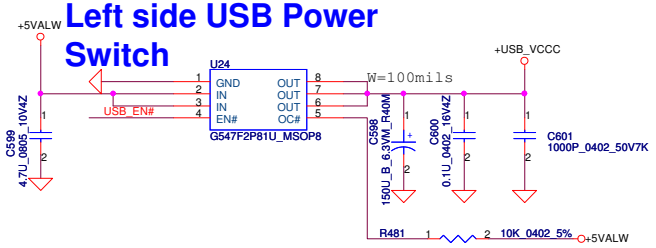
Audio/B & CIR



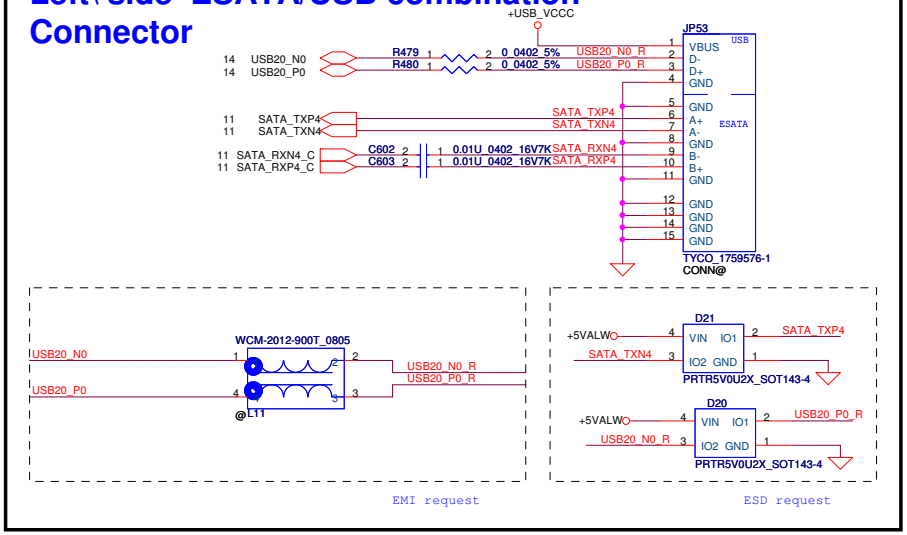
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Title	AMP & Audio Jack		
Size Custom	Document Number	Calpella_UMA_LA4106P	Rev 1.0
Date: Thursday, November 12, 2009	Sheet 28 of 45		

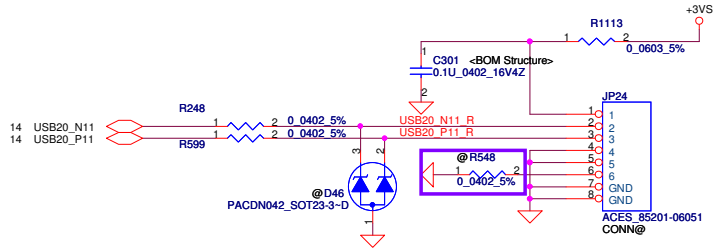
Left side USB Power Switch



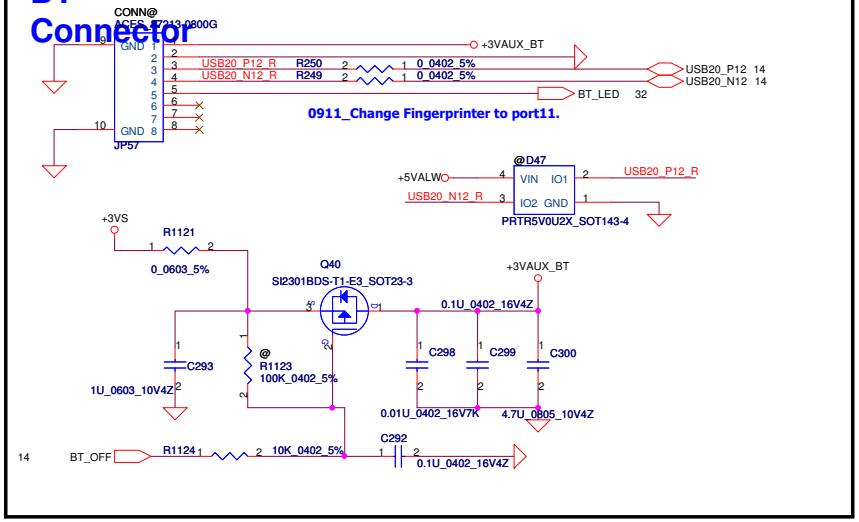
Left\ side ESATA/USB combination Connector



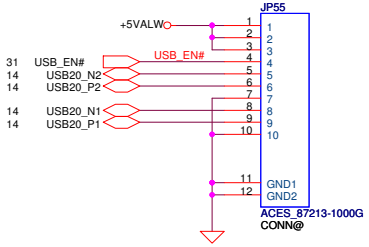
Finger printer



BT Connector



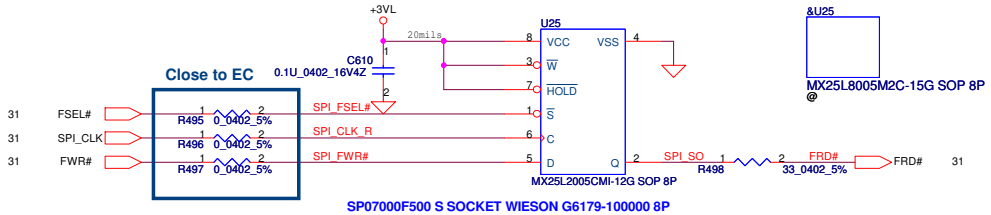
USB cable connector for Right side



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: USB, BT, eSATA			
Size	Document Number: Calpella_UMA_LA4106P		Rev: 1.0
Date: Thursday, November 12, 2009	Sheet 29 of 45		

SPI ROM => 256K (EC code)

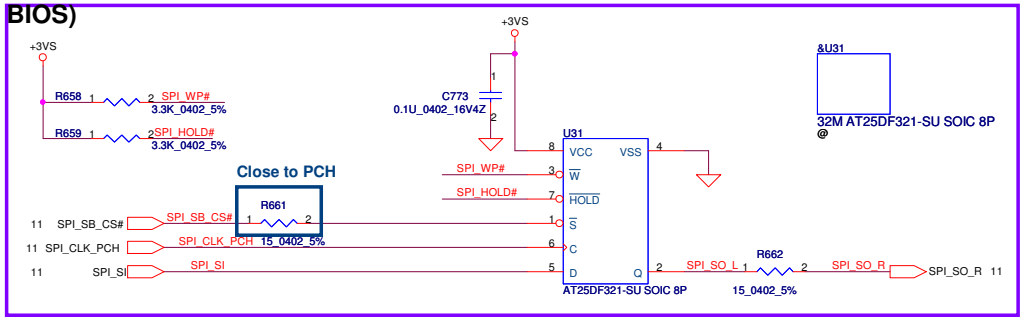


SP07000F500 S SOCKET WIESON G6179-100000 8P
SPIFLASH
WIESO_G6179-100000_8P

★ SA00003GK00 S IC FL 2M MX25L2005CMI-12G SOP 8P
(MXIC)

SA00003GM00 S IC FL 2M W25X20AVSNIG SOIC 8P
(WINBOND)

SPI ROM on PCH => 4M (ME code + System BIOS)



★ SA000031Q00 S IC FL 32M AT25DF321-SU SOIC 8P
(ATMEL)

SA000021A00 S IC FL 32M MX25L3205DM2I-12G SOP 8P
(MXIC)

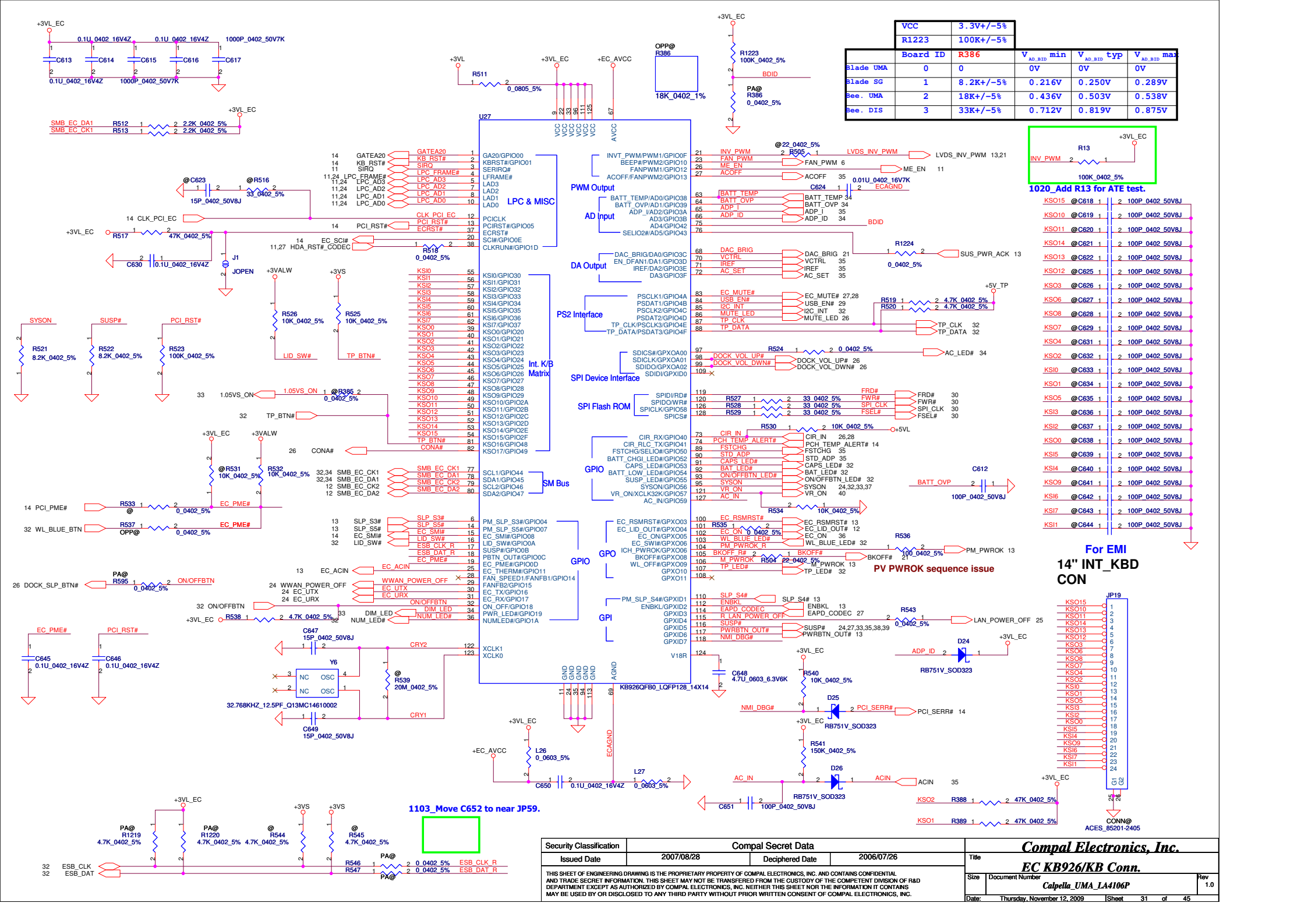
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: BIOS ROM

Size | Document Number: Calpella_UMA_LA4106P | Rev: 1.0

Date: Thursday, November 12, 2009 | Sheet 30 of 45



	VCC	3.3V+/-5%
	R1223	100K+/-5%

	Board ID	R386	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
Blade UMA	0	0	0V	0V	0V
Blade SG	1	8.2K+/-5%	0.216V	0.250V	0.289V
Bee. UMA	2	18K+/-5%	0.436V	0.503V	0.538V
Bee. DIS	3	33K+/-5%	0.712V	0.819V	0.875V

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

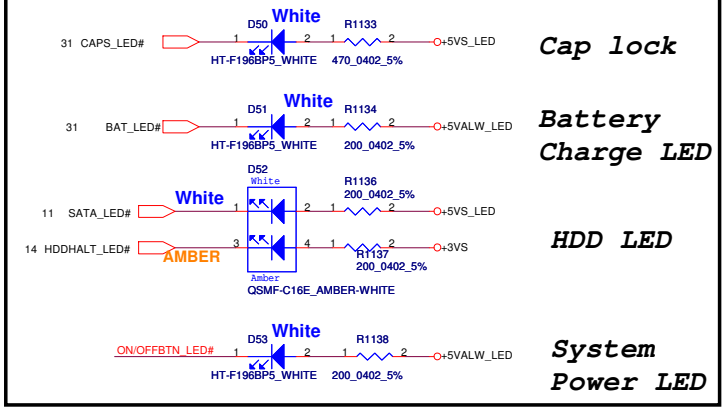
Compal Electronics, Inc.

Title: EC KB926/KB Conn.

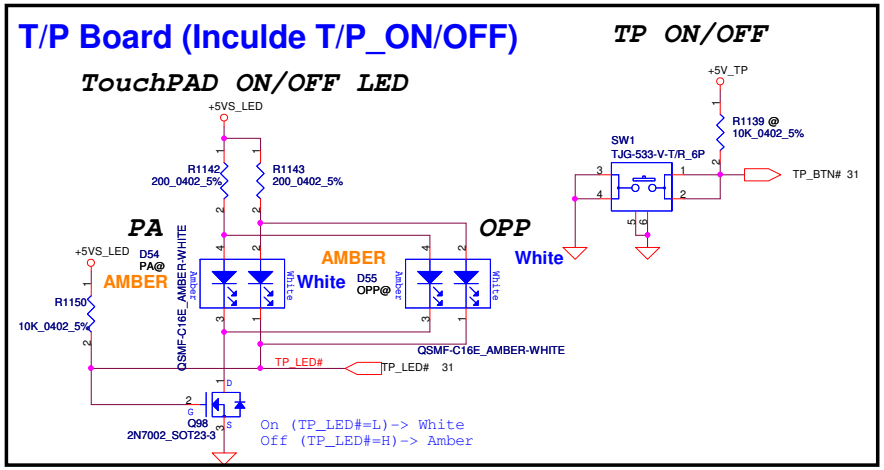
Size	Document Number	Rev
	Calpella_UMA_LA4106P	1.0

Date: Thursday, November 12, 2009 Sheet 31 of 45

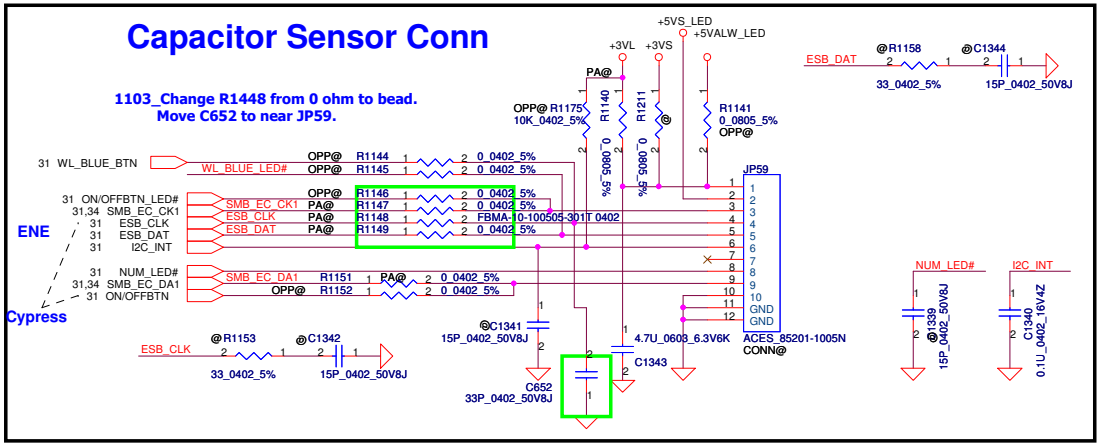
System & Caps-Lock LED



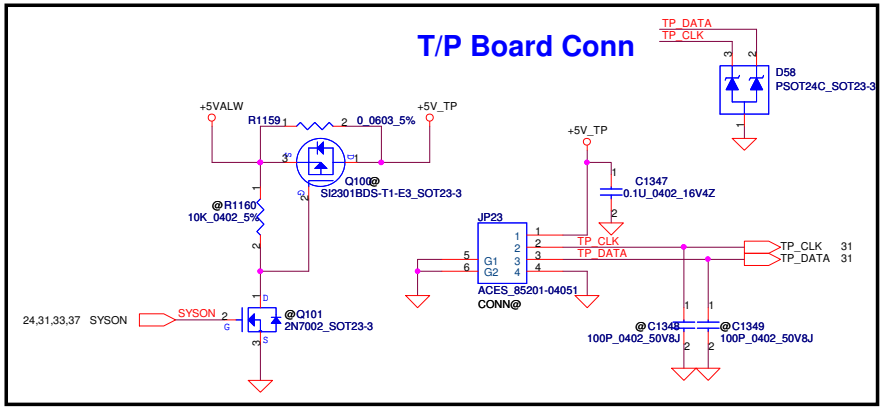
T/P Board (Inculde T/P_ON/OFF)



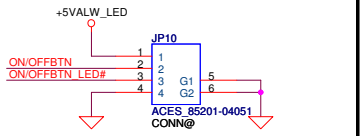
Capacitor Sensor Conn



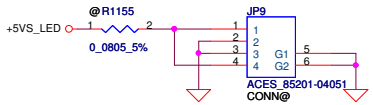
T/P Board Conn



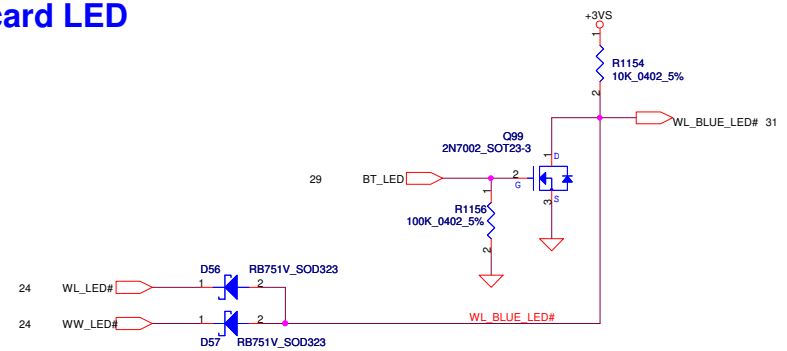
ON/OFF Button Connector



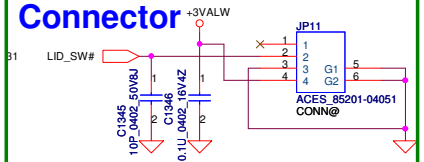
Keyboard backlight Conn



Mini card LED



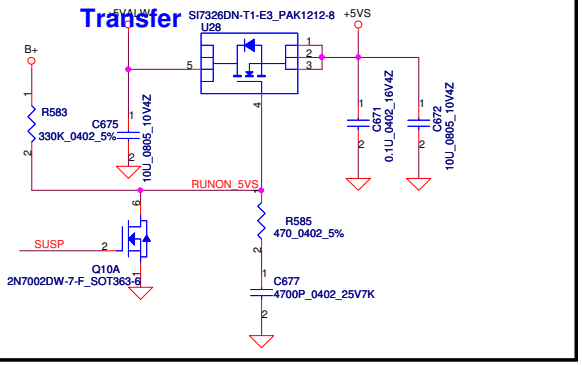
Lid Switch Connector



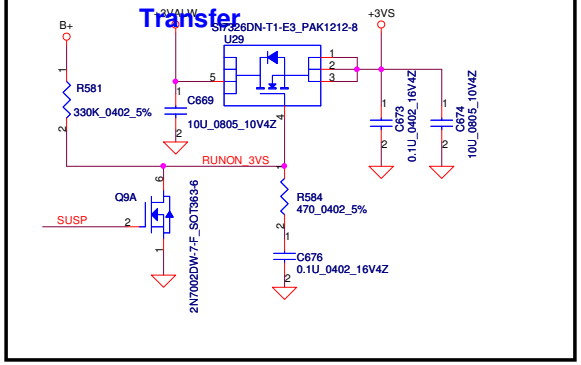
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title	KBD, ON/OFF, SW, CIR		
Size	Document Number	Rev	
	Calpella_UMA_LA4106P	1.0	
Date: Thursday, November 12, 2009	Sheet 32 of 45		

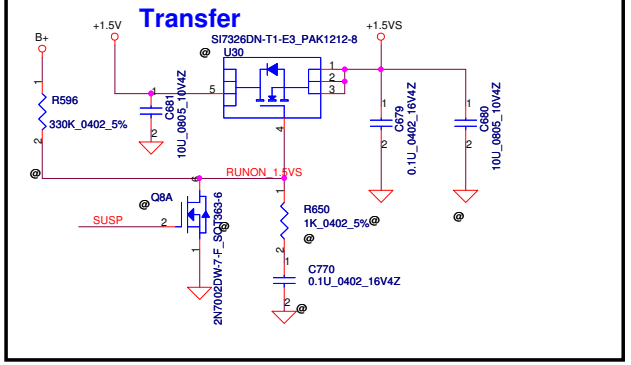
+5VALW to +5VS Transfer

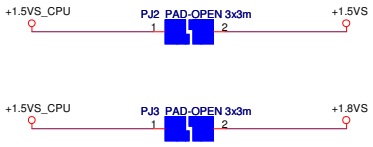


+3VALW to +3VS Transfer

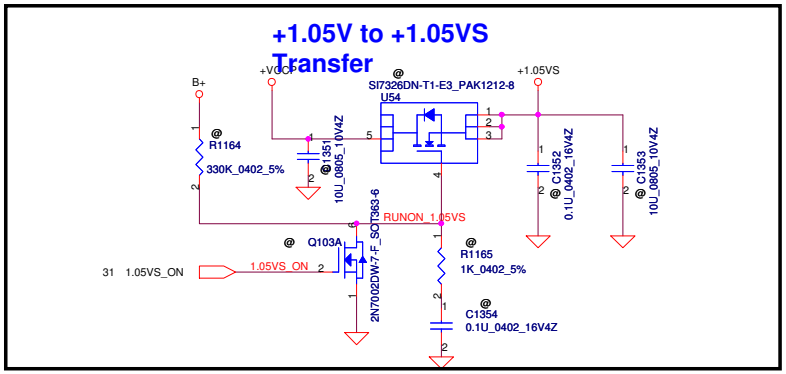


+1.5V to +1.5VS Transfer





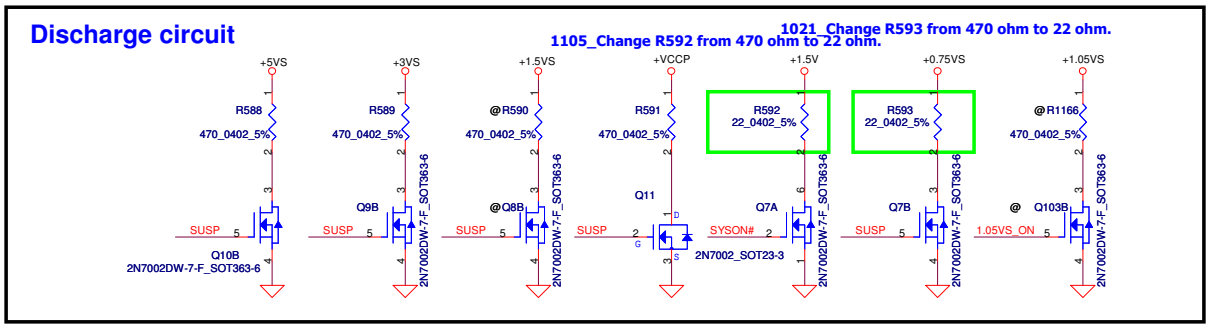
+1.05V to +1.05VS Transfer

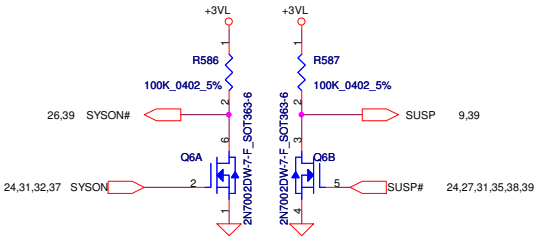


Discharge circuit

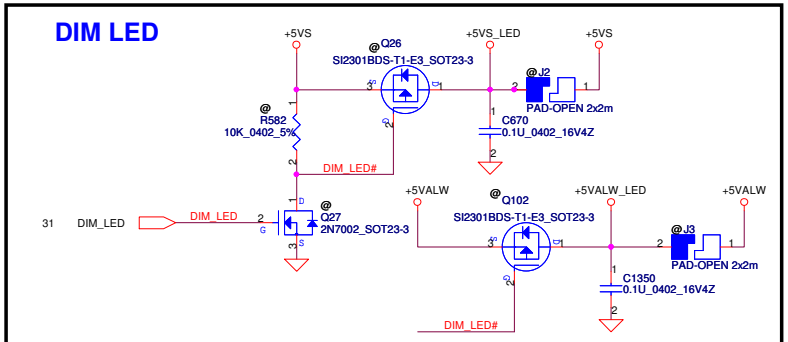
1105_Change R592 from 470 ohm to 22 ohm.

1021_Change R593 from 470 ohm to 22 ohm.





DIM LED



H1 HOLEA H2 HOLEA H3 HOLEA H4 HOLEA H5 HOLEA H6 HOLEA H7 HOLEA H8 HOLEA H9 HOLEA H10 HOLEA H15 HOLEA H16 HOLEA H17 HOLEA H18 HOLEA H19 HOLEC H20 HOLEC H11 HOLEA FM1 FM2 FM3 FM4

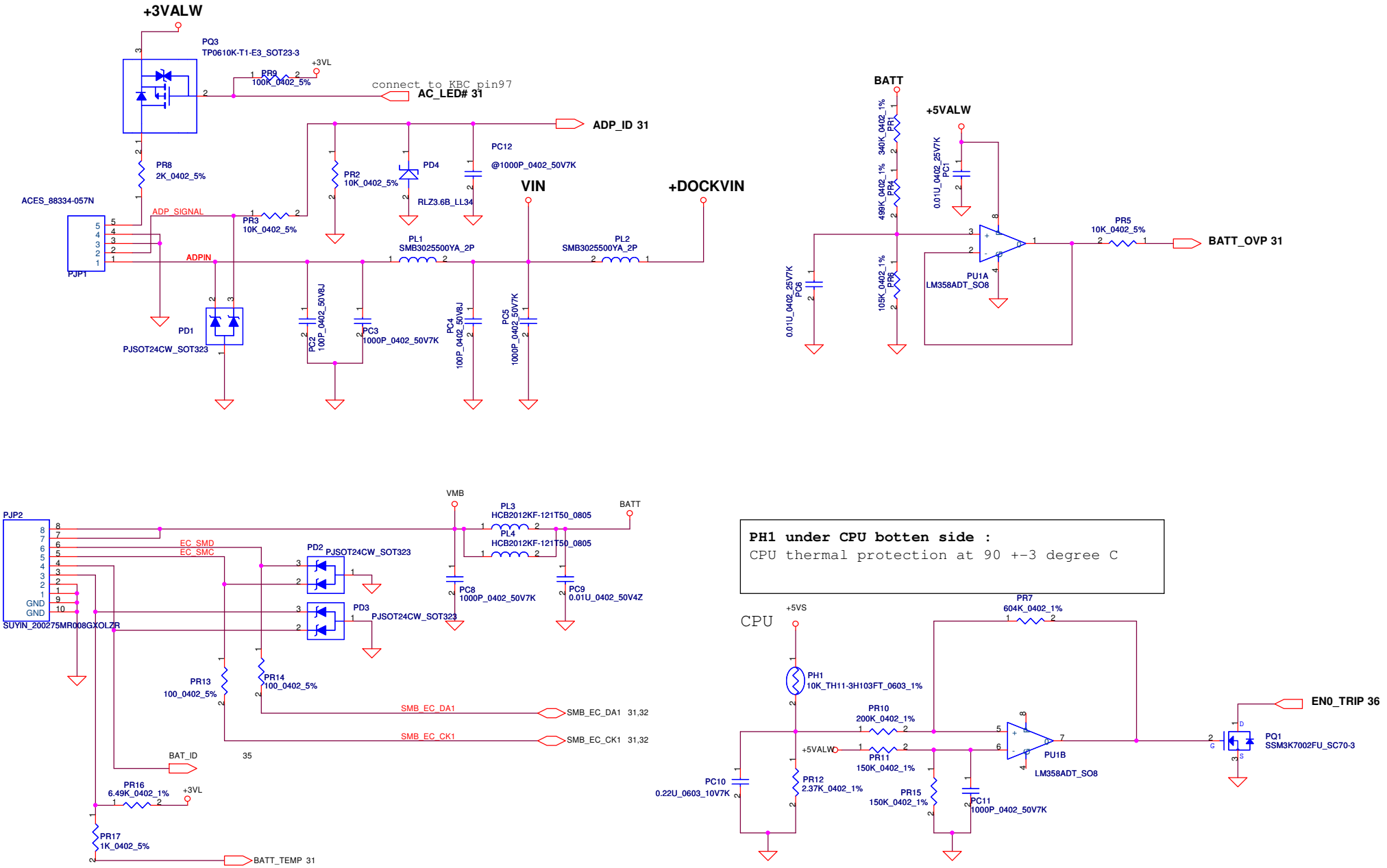
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: DC/DC Interface

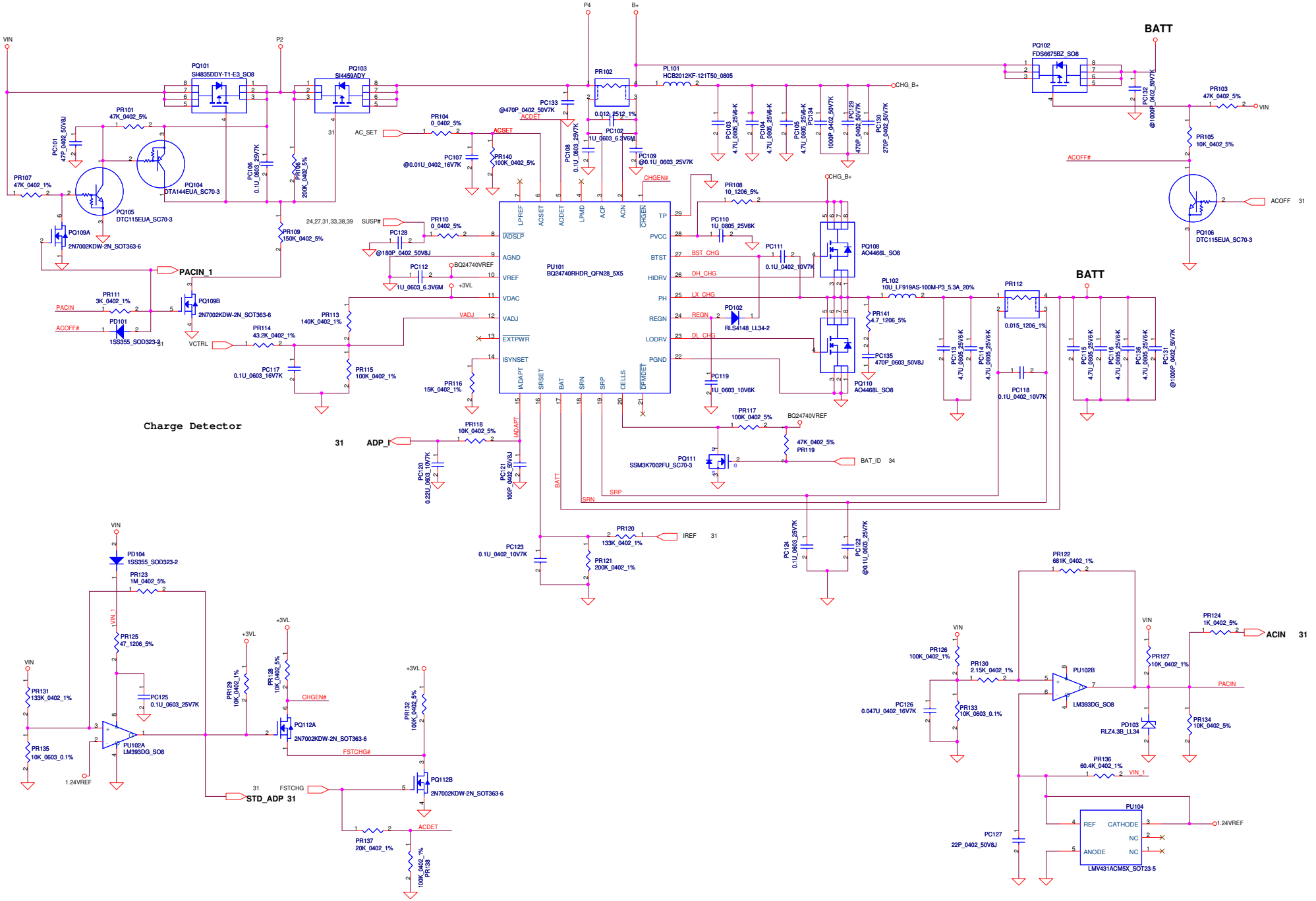
Size | Document Number: Calpella_UMA_LA4106P | Rev: 1.0

Date: Thursday, November 12, 2009 | Sheet 33 of 45



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.			
Title	DC Connector/CPU_OTP		
Size	Document Number: Calpella_UMA_LA4106P		Rev: 0.3
Date: Thursday, November 12, 2009	Sheet 34 of 45		



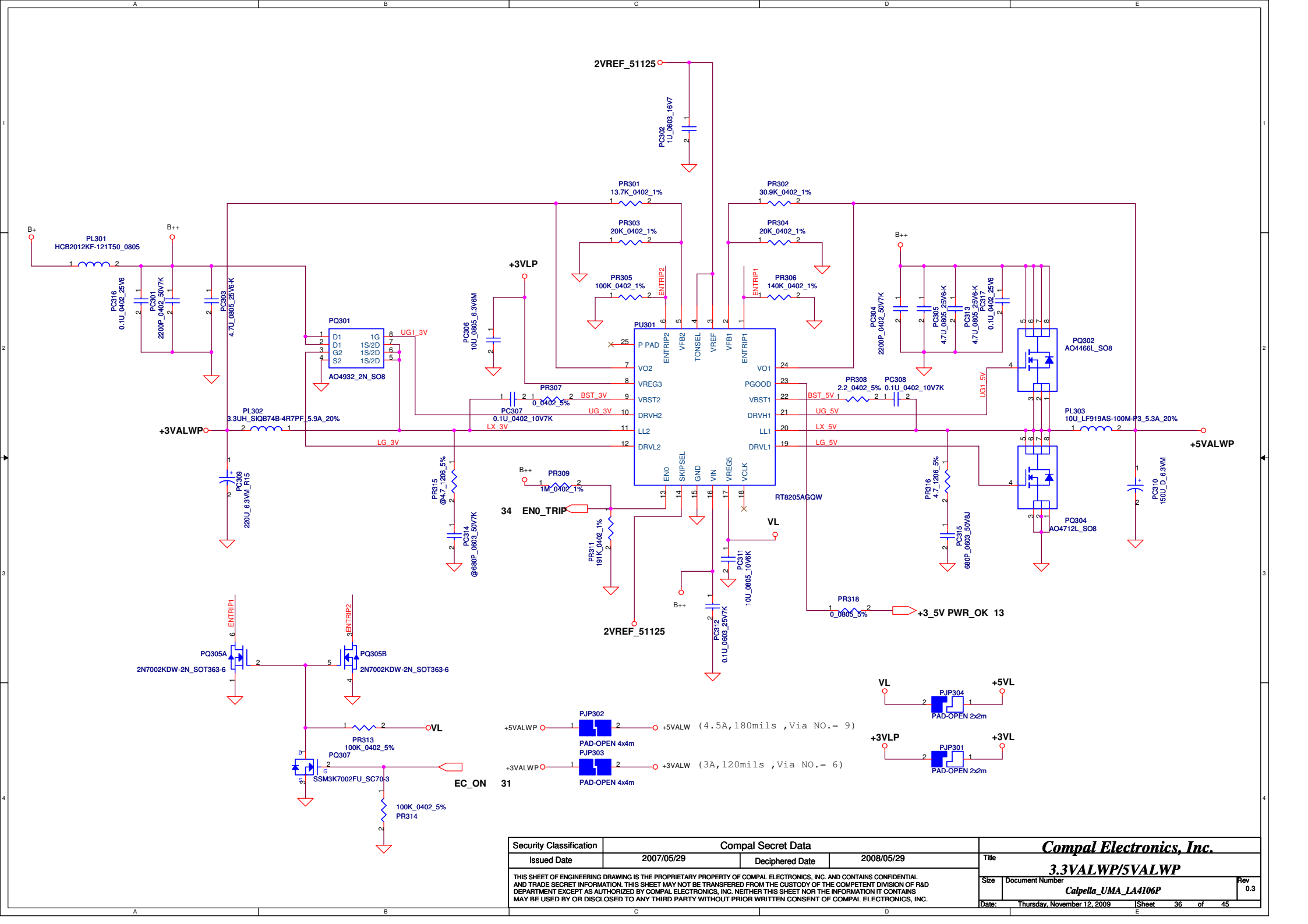
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **Charger**

Size	Document Number	Rev
	Calpella_UMA_LA4106P	0.3

Date: Thursday, November 12, 2009 | Sheet 35 of 45



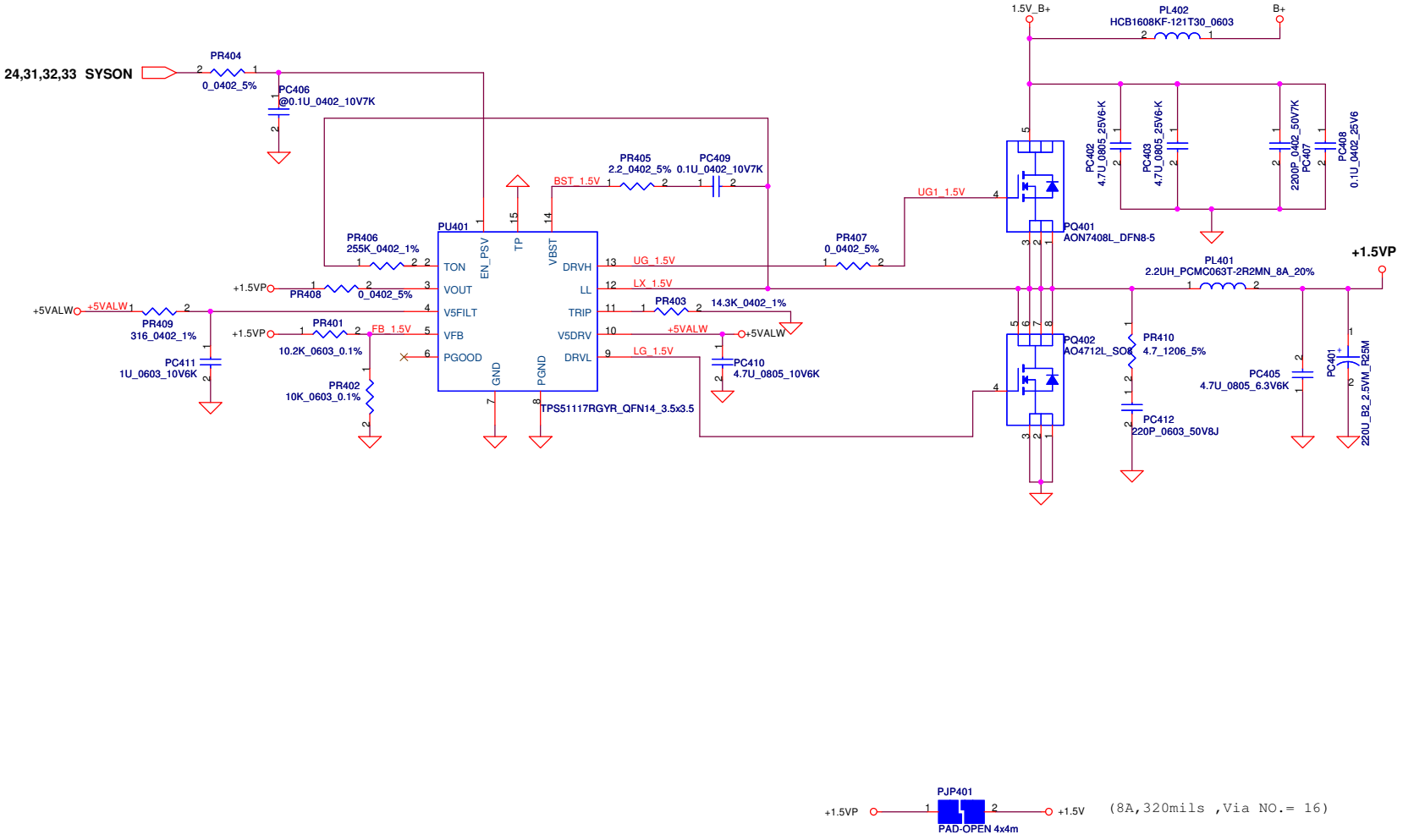
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

Size	Document Number	Rev
	Calpella_UMA_LA4106P	0.3

Date: Thursday, November 12, 2009 | Sheet 36 of 45



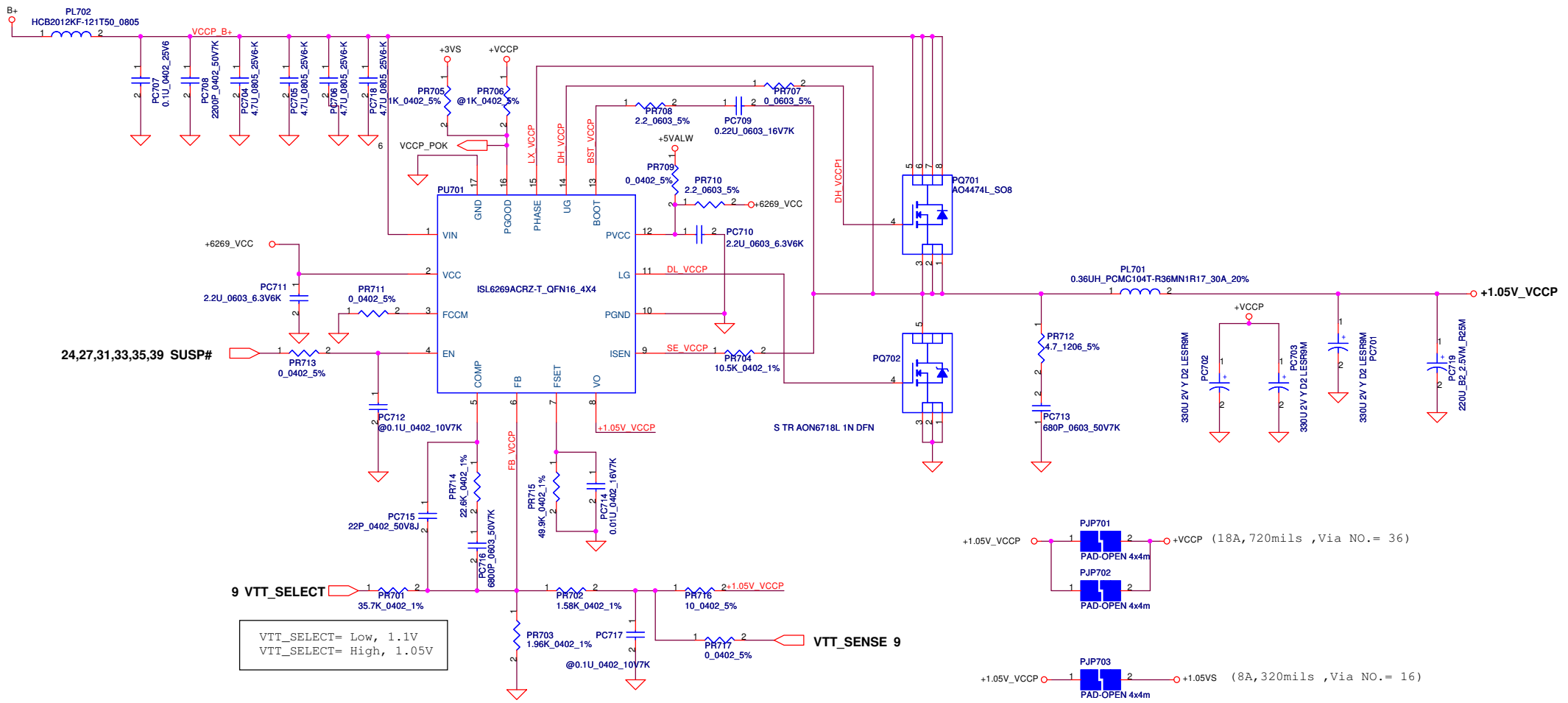
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **+1.5VP**

Size	Document Number	Rev
	Calpella_UMA_LA4106P	0.3

Date: Thursday, November 12, 2009 | Sheet 37 of 45



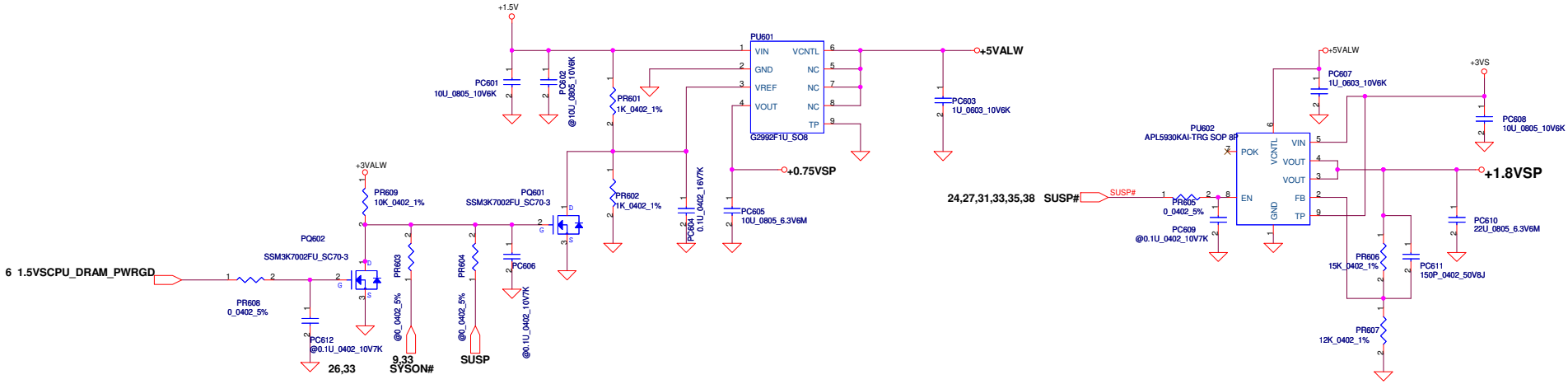
Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

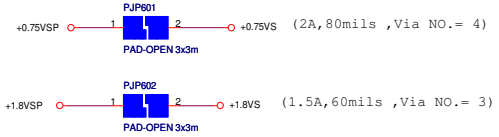
Compal Electronics, Inc.

Title: **1.05V_VCCP**

Size	Document Number	Rev
	Calpella_UMA_LA4106P	0.3

Date: Thursday, November 12, 2009 | Sheet 38 of 45





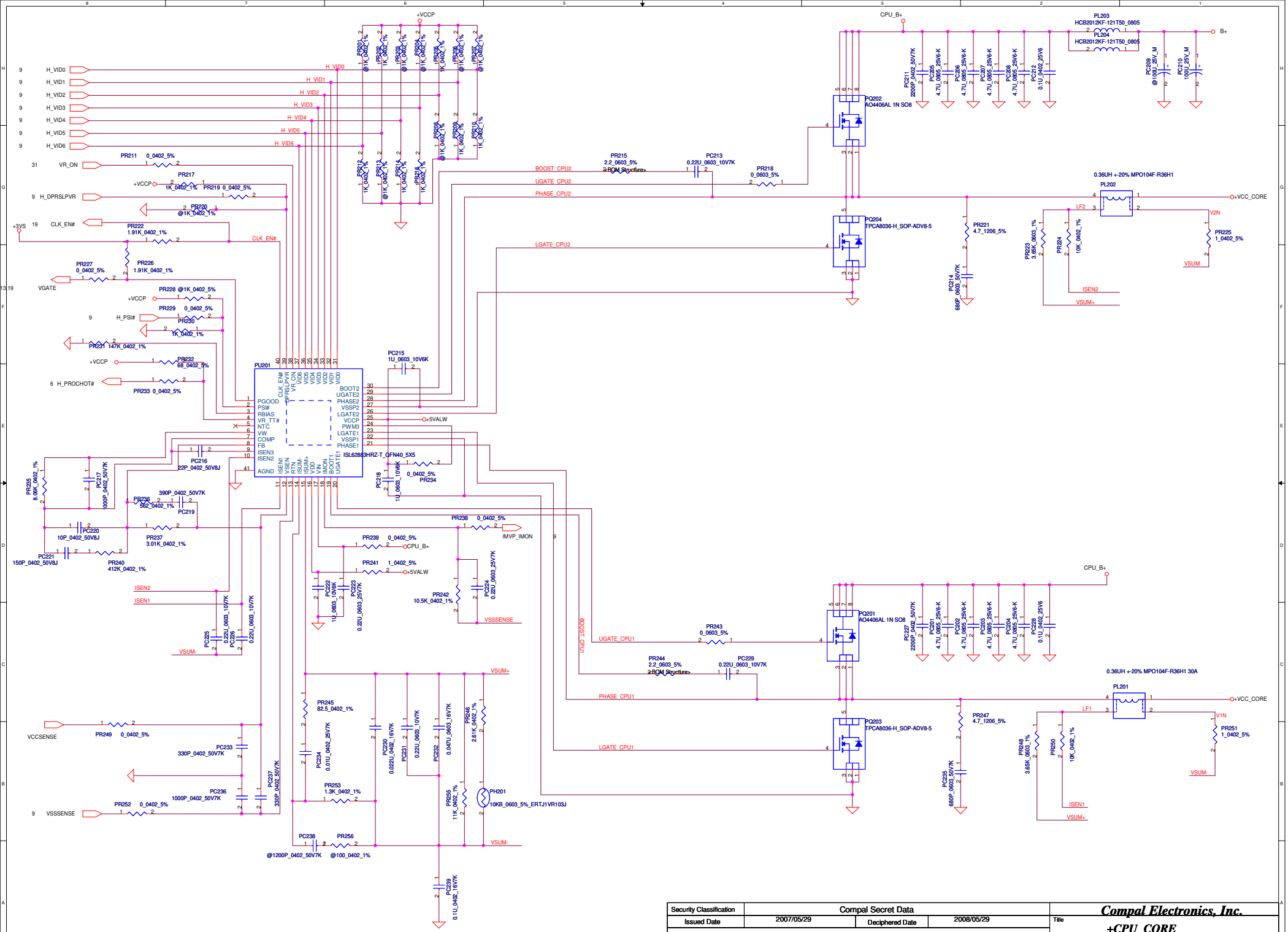
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: 0.75VP/1.8VSP

Size | Document Number: Calpella_UMA_LA4106P | Rev: 0.3

Date: Thursday, November 12, 2009 | Sheet 39 of 45



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

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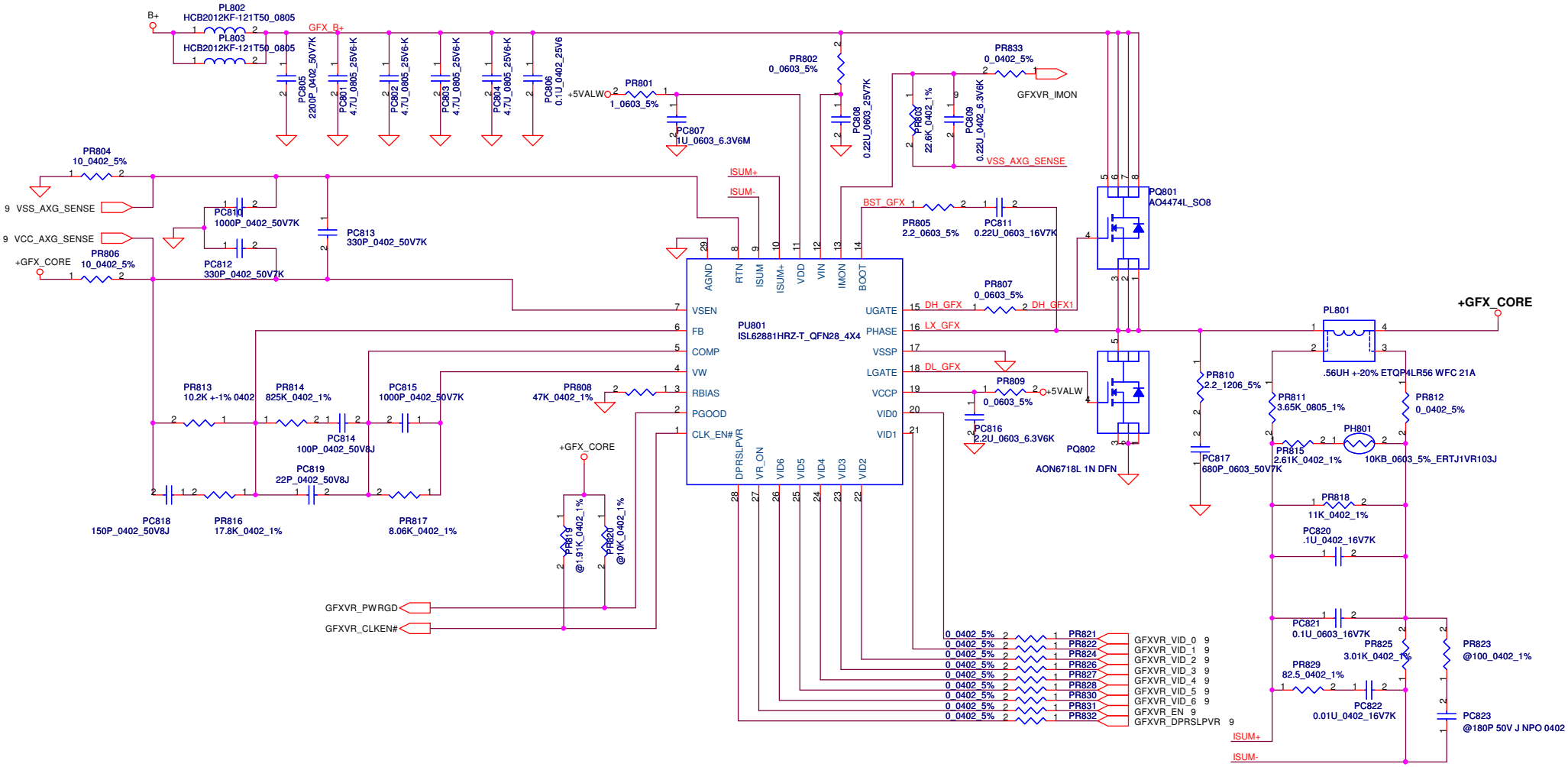
Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
	Calpella_UMA_LA4106P	0.3
Date: Thursday, November 12, 2009	Sheet 40 of 45	



Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: **VCCGFX**

Size	Document Number	Rev
Custom	Calpella_UMA_LA4106P	

Date: Thursday, November 12, 2009 | Sheet 41 of 45

Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Note
1	36	PWR-3.3VALWP/5VALWP	8/12	PWR	all cap no more than 0805	Add PC313,PC305 from 1206 to 0805 and parallel PC313	DB to PV1
2	40	PWR-CPU_CORE	8/13	PWR	OCP & IMON ajustment and Fixed LL to match INTEL Spec	Change PR253 from 1.1K to 1.3K,Change PR242 from 8.25K to 10.5K Change PR237 from 2.43K to 3.01K	DB to PV1
3	40	PWR-CPU_CORE	8/17	PWR	RF Solution	Change PQ201 PQ202 from AO4474L to AO4406AL	DB to PV1
4	39	PWR-0.75VP/1.8VSP	8/20	PWR	Cost Down plan	Change PU602 from APL5915 to APL5930	DB to PV1
5	35	PWR-Charger	8/20	PWR	Smart Charger	Change PR113 from 143K to 140K, Change PC117 from 1u to 0.1u, Add PR114	DB to PV1
6	38	PWR-1.05V_VCCP	8/24	PWR	Follow HW Suggestion Pull-up resistor connect to 3VS	Add PR705 connect to 3VS, remove PR706	DB to PV1
7	37	PWR-1.5VP	8/24	PWR	PU401 second source solution	PR403 from 8.45K to 14.3K	DB to PV1
8	38	PWR-1.05V_VCCP	8/24	PWR	PU701 second source solution	PR703 from 8.25K to 10.5K	DB to PV1
9	40	PWR-CPU-CORE	8/28	PWR	Improve transient response	Add PC230	DB to PV1
10	38	PWR-1.05V_VCCP	9/2	PWR	Cost down plan	PQ702 from TPCA8028-H to AON6718L	DB to PV1
11	38	PWR-1.05V_VCCP	9/3	PWR	Improve VCCP Ripple	Delet PC717	DB to PV1
12	41	GFX_CORE	9/11	PWR	Let GFX IMON measure easily	Add PR833 connet to GFXVR_IMON and PU801 13pin	PV1 to PV2
13	39	PWR-0.75VP/1.8VSP	9/11	PWR	For HW requirement add 1.5VSCPU_DRAM_PWRGD	Add 1.5VSCPU_DRAM_PWRGD add PR608 connect to PQ601 pin 2 and Delet PR604	PV1 to PV2

Item	PAGE	Fixed Issue	Request by	Modify List	Date	Note
01	22		HW	Add R801	7/20.	DB --> PV-1
02	26	Fix Volum up/down cannot work on Docking.	HW	Add R1185, R1186 and pull high to +3VS.	7/20.	DB --> PV-1
03	31	Remove double pull high resistor.	HW	Delete R660.	7/20.	DB --> PV-1
04	13	Per EMI request.	EMI	Change R679 from 33 ohm to 100 ohm.	7/20	DB --> PV-1
05	31	Modify correct pull high resistor value.	HW	Change R512 and R513 from 4.7K to 2.2K ohm.	7/20	DB --> PV-1
06	32	Modify LVDS PWM connection.	HW	Connect R890 to PCH and R505(reserve) to EC.	7/24	DB --> PV-1
07	22	Fix cannot hot plug if use Asmedia level shifter.	HW	Remove R862 and R867.	8/13	DB --> PV-1
08	22	Add series for Express card delete signal between Express card power swtich and PCH	HW	Add R1210	8/13	DB --> PV-1
09	31	For Board ID.	HW	Add R386 and pull low to GND.	8/13	DB --> PV-1
10	31	Change LAN power off control pin to U27 pin115.	HW	Connect U27 pin115 and add series resistor R543 to LAN power control circuit.	8/13	DB --> PV-1
11	31	Change LID switch power rail from +3VL to +3VALW.	HW	Pull high R526 to +3VALW.	8/13	DB --> PV-1
12	31	Delete useless parts.	HW	Delete R542 because already connect EC_UTX to MINI PCIE connector	8/13	DB --> PV-1
13	32	Change LID switch power rail from +3VL to +3VALW.	HW	Change JP11 pin 1 to +3VLALW.	8/13	DB --> PV-1
14	33	For Cost down.	HW	Reserve U30, R596, R650, R590, C681, C770, C679, C680, Q8; add PJ2 to connect +1.5VS_CPU and +1.5VS power plan.	8/13	DB --> PV-1
15	33	Try to use +1.5VS to replace +1.8VS power rail.	HW	Add and reserve PJ3 to short +1.8VS and +1.5VS_CPU power plan.	8/13	DB --> PV-1
16	14	Modify prevent S3 leakage issue circuit.	HW	Connect PCH_DDR_RST from EC GPIO48 to PCH GPIO46.	8/13	DB --> PV-1
17	31	Modify prevent S3 leakage issue circuit.	HW	Delete R386	8/13	DB --> PV-1
18	21	Fix LCD panel no display issue.	HW	Connect JLVDS1 pin27 to +3VS.	8/13	DB --> PV-1
19	32	Change Cap. board power rail from +3VL to +3VS.	HW	Reserve R1211 and connect to +3VS.	8/13	DB --> PV-1
20	27	Swap Audio port A and F.	HW	Swap port A and port F. Detail please see audio circuit.	8/17	DB --> PV-1
21	6	Delete XDP connector	HW	Delete JP1, R13, R17, R18, R19, R22, R25, C1	8/17	DB --> PV-1
22	25	Conecto Q15 to +3V_LAN.	HW	Delete R1031 and connect Q15 pin1 to +3V_LAN directly.	8/17	DB --> PV-1
23	26	Modify Audio circuit near docking side.	HW	Connect Q91 pin3 to GNDA and move it near Codec.	8/17	DB --> PV-1
24	27	Per EMI/ESD request.	EMI/ESD	Add R1212/C1433 for HDA_RST#_CODEC. Add C1434. Change R132/R135/R139 to C1435/C1436/C1437.	8/17	DB --> PV-1
25	6	Modify prevent S3 leakage issue circuit.	HW	Change U57 from reset IC to AND gate; add R1218 and reserve R383; add voltage divider(R1216/R1217) for VTTPWRGOOD.	8/19	DB --> PV-1
26	25	Follow DIS.	HW	Change Y8 material.	8/19	DB --> PV-1
27	28	Per ESD request.	ESD	Add D61, D62 for OPP sku.	8/19	DB --> PV-1
28	32	Change cap. board power rail from +3VL to +3VS.	HW	Pull high R544 and R545 to +3VS power rail.	8/20	DB --> PV-1
29	14	Make sure PLT_RST# level is stable.	HW	Stuff R185.	8/20	DB --> PV-1
30	32	Reserve +3VL power rail for cap. board.	HW	Add and reserve R1219/R1220 to +3VL.	8/21	DB --> PV-1

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Item	PAGE	Fixed Issue	Request by	Modify List	Date	Note
01	6	Make sure +1.5VS can ramp up early than +0.75VS.	HW	Connect 1.5VSCPU_DRAM_PWRGD to enable PU601.	9/11	PV-1 --> PV-2
02	11	ME fuction control enable/disable.	SW/EC	Add Q106, R1221, R1222 and connect to EC pin26.	9/11	PV-1 --> PV-2
03	13	For support ME function.	SW/EC	Connect SUS_PWR_ACK to EC pin76.	9/11	PV-1 --> PV-2
04	14	HM55 disable USB port6/port7.	INTEL	Change Bluetooth port6 to port12, change Fingerprinter port7 to port11.	9/11	PV-1 --> PV-2
05	27	To solve no Vref out when external MIC change from port A to port F.	HW	Reserve R431, add R and connect to +AVDD_CODEC.	9/11	PV-1 --> PV-2
06	27	Delete EC_BEEP from EC because useless.	HW	Delete EC_BEEP to EC.		
07	28	Delete ANA_MIC_DET net to EC.because useless.	HW	Delete ANA_MIC_DET to EC.	9/11	PV-1 --> PV-2
08	29	HM55 disable USB port6/port7.	INTEL	Change Bluetooth port6 to port12, change Fingerprinter port7 to port11.	9/11	PV-1 --> PV-2
09	31	Board ID is not enough when use pin81.	EC	Swap TP_BTN# and BDID, then add pull high resistor R1223 for BDID.	9/11	PV-1 --> PV-2
10	31	ME fuction control enable/disable.	SW/EC	Remove EC_BEEP and change to ME_EN, then connect ME_EN to Q106.	9/11	PV-1 --> PV-2
11	31	For support ME function.	SW/EC	Remove ANA_MIC_DET and change to SUS_PWR_ACK, then connect SUS_PWR_ACK to PCH.	9/11	PV-1 --> PV-2
12	31	Chagne ENE cap. board ESB bus power rail from +3VS to +3VL.	HW	Reserve R544/R545 and stuff R1219/R1220.	9/11	PV-1 --> PV-2
13	32	Chagnge Cap. board power rail from +3VS to +3VL.	HW	Reserve R1211 and stuff R1140.	9/11	PV-1 --> PV-2
14					9/11	PV-1 --> PV-2

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01	12	To solve RTL8401 cause BSOD 0xD1 issue.	HW	Change RTL8401 PCIE port from port3 to port5 (follow Rhett2.0), new add series resistor R506/0 ohm.	10/19	Delete this item in 10/26.
02	12	To solve HDMI signal jitter fail issue.	Intel	Add Y2, R131, C141. Change C142 from 0 ohm to 18pF.	10/19	PV-2 --> MV
03	19	To solve time too fast in DOS mode.	HW	Change R259 and R260 from 18pF to 22pF.	10/19	PV-2 --> MV
04	25	To solve RTL8401 cause BSOD 0xD1 issue.	HW	Change RTL8401 PCIE port from port3 to port5 (follow Rhett2.0)	10/19	Delete this item in 10/26.
05	31	To solve cannot power on when no CPU insert in ATE test.	HW	Add pull high resistro R13 to +3VL_EC for EC pin21.	10/20	PV-2 --> MV
06	33	To meet Intel power down sequence spec.	HW	Change R593 from 470 ohm to 22 ohm.	10/21	PV-2 --> MV
07	09	To meet Intel power down sequence spec.	HW	Change R1182 from 470 ohm to 220 ohm.	10/21	PV-2 --> MV
08	13	Follow Intel schematic checklist rev2.0 change.	HW	Change R137 from 1K ohm to 10K ohm.	10/21	PV-2 --> MV
09	27	To solve audio noise issue.	HW	Add and reserve U59, R1228, C1443, C1444, C1445, C1446, R1226, R1227.	11/02	PV-2 --> MV
10	04	To solve ESD test fail.	ESD	Add and reserve C1438, C1439, C1440 near Q104.	11/03	PV-2 --> MV
11	17	To solve ESD test fail.	ESD	Add and reserve C1441 near JDIMM1.	11/03	PV-2 --> MV
12	18	To solve ESD test fail.	ESD	Add and reserve C1442 near JDIMM2.	11/03	PV-2 --> MV
13	28	To solve ESD test fail.	ESD	Add and reserve C1447 between GND and GNDA near internal MIC connector.	11/03	PV-2 --> MV
14	32	To solve EMI test fail.	EMI	Change R1148 from 0 ohm to bead (SM01000CY00), move C652 to near JP59.	11/03	PV-2 --> MV
15	32	To solve EMI test fail.	EMI	Move C652 to near JP59.	11/03	PV-2 --> MV
16	27	To solve audio noise issue.	EMI	Move C652 to near JP59.	11/03	PV-2 --> MV
17	27	Reserve ref. power for external MIC.	HW	Reserve R1230 to connect +VREFOUT_INMIC.	11/05	PV-2 --> MV
18	27	To solve GFX power spike when S0 to S3/S5.	Intel	Change R43 from 4.7K ohm to 249 ohm.	11/05	PV-2 --> MV
19	33	To meet Intel power down sequence spec.	HW	Change R592 from 470 ohm to 22 ohm.	11/05	PV-2 --> MV
20	6	To reduce powr noise from FAN.	HW	Add R597.	11/05	PV-2 --> MV

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